University of Alberta

On-Line Current Monitoring of Low-Voltage VLSI Circuits

by

Ivan Pecuh

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of **Master of Science**.

Department of Electrical and Computer Engineering

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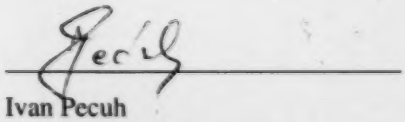

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Abstract

This thesis presents the designs for two on-line current monitors for testing of VLSI circuits. Both monitors are designed to operate in a low-voltage environment with 1.5 Volts power-supply. The first design (Monitor 1) is an improvement of the Stopjavová/Manhaeve design, and the second one (Monitor 2) is a new proposed monitor scheme with two current-sensing elements. These designs can be used in quiescent current-monitoring—Iddq, and transient-current monitoring—Iddt. The second design can also be used in tesing of mixed-signal VLSI circuits. The simulation test results of the two monitors demonstrate an ability to detect a short and an open fault in a circuit-under-test.

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Chapter 1

Introduction

The testing of integrated circuit (IC) designs is gaining in importance every day. This is understandable since better testing implies higher quality. Low quality products can ultimately have a negative impact on society through the cost of their development, maintenance and repair. With the continuing advances in the manufacturing of IC technology, testing constitutes a large portion of the total cost. Decreasing silicon costs, together with the increased complexity of integrated circuits present two of the most important elements of this trend [1]. It is expected that chips with 100-milion transistors will emerge in the near future [2]. Market-driven developments in the area of wireless communications lead to the emergence of complex mixed-signal (analog-digital) circuits and indicate a trend toward the integration of the radio frequency (RF) and baseband mixed-signal technologies. In addition, submicron design techniques and low-power designs demand an improvement in fault coverage and the necessity for development of new testing techniques.

1.1 Testing in IC Manufacturing

Testing has two important functions in the process of IC manufacturing. One is the go/no-go testing used during the manufacturing process and the other is defect analysis done during diagnosis. Go/no-go testing is done repeatedly in several steps [3]. Wafers, dice, and chips are probed and tested to screen devices that fail performance specifications under specified conditions. Figure 1.1 describes the major steps in the IC manufacturing process, together with the points where IC testing is performed. A bad device is considered to be any IC that fails to meet one or more specifications at any point in the process. Each of the steps has different issues and requirements.

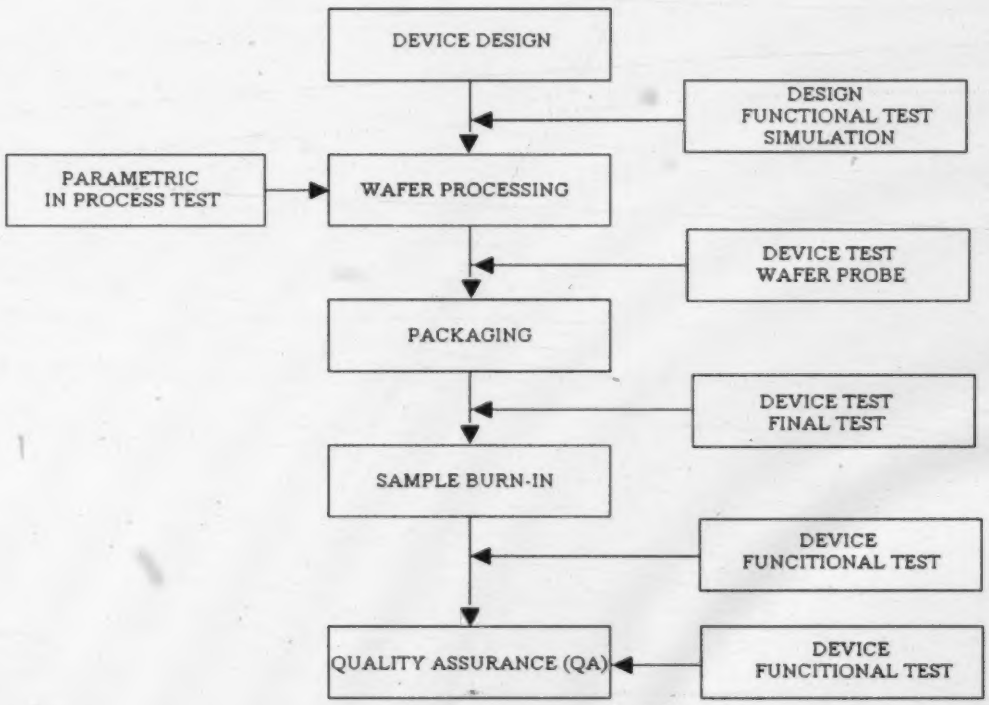

Figure 1.1: Major steps in IC manufacturing process

Initially, when a design is developed using computer-aided-design (CAD) tools, a designer verifies desired functionality through simulations. During the processing of wafers, parametric tests are performed to evaluate process control. At the end of the wafer processing, functional tests are used to eliminate faulty devices. This is commonly referred to as the "test suite." It identifies any catastrophic process control errors. At this point, wafer probing can be done either by using a complete set of tests needed for a particular design or only a subset of tests. Bad devices are marked, and the wafer is ready for scribing. Good dies are selected for packaging. After a packaging, a final test is performed to ensure proper handling, bond wiring and packaging. The performance of the device is checked over the specific temperature range it will function in. In the next step, a sample burn-in test is performed only on a selected set of IC's. This is done using a higher temperature for an extended period of time. The initial part of the so-called "bath-tub curve" describes the failure behavior of devices in the early period of operation. Before the delivery of the product to the customer, the Quality Assurance (QA) test has to be performed. The need for standardization of the QA test was driven by globalization in the microelectronics industry, resulted in two popular ISO9000 and ISO9001 standards.

The main purpose of apparently redundant tests is to increase the probability of detection of bad devices in the early stages of the manufacturing process. The "factor of ten" rule is used in describing the costs resulting from the production of bad devices. Every additional step that a bad device reaches without detection multiplies the original cost of production by a factor ten. If a faulty device reaches the market, it leads to a damaged reputation and ultimately to a loss of market share.

1.2 Aspects of IC Testing

Increasing complexity increases the probability of bad devices, reducing the yield. Yield is defined as the ratio of good devices over the total number of devices fabricated. Increased complexity also introduces new challenges to the testing of IC's. The International Technology Roadmap of Semiconductors (ITRS), produced by the

Semiconductor Industry Association (SIA) [4], predicts a rapid increase in the number of transistors per pin (Figure 1.2). The testing complexity index, as shown in this graph, predicts rapid decrease in the accessibility of transistors from the chip pins. This presents one of the biggest problems in IC testing.

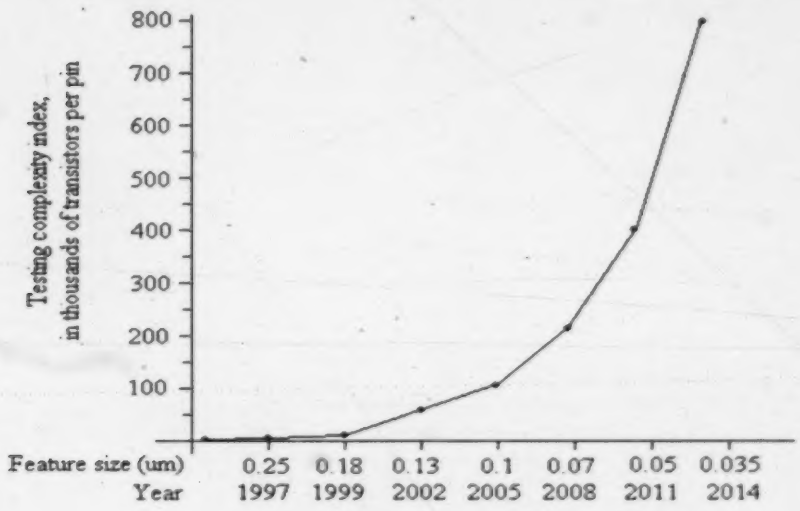

Figure 1.2: Testing complexity index

Another major problem in IC testing is the gap between internal performance and output capabilities of the input/output (I/O) link. The difference between the internal clock speed and external capabilities of the IC chip constantly increases and creates the problem of interaction between the two media, rendering at-speed testing of IC performance almost impossible. The I/O bandwidth lags far behind the speed at which the information can be generated and moved inside or outside the chip. This gap, as analyzed in SIA Roadmap for the next 14 years is shown in Table 1.1. External bandwidth, defined as number of I/O's times I/O switching speed, does not follow the internal bandwidth at the same rate. Internal bandwidth is basically the speed at which the chip can generate and process information, and it is defined as the number of transistors per IC times internal switching frequency.

Table 1.1: Bandwidth gap prediction (Source: 1998 SIA Roadmap)

BANDWIDTH:							
Internal	1	3.165	19.52	85.26	375.35	1621.62	7132.76
External	1	1.97	3.59	6.14	10.5	17.24	28.89
	1997	1999	2002	2005	2008	2011	2014

1.3 IC Testing Methodologies

Generally, IC testing methodologies can be classified into two categories: voltage testing and parametric testing. The first analyzes logic levels of the circuit-uder-test (CUT) outputs. The CUT is a generic term used in the literature to refer to the integrated circuit design or component being tested. After the input stimuli have been applied to the CUT, circuit response is compared with the logic values produced by the reference circuit for the same input stimuli. The second one is concerned with the values of CUT parameters such as power supply current, propagation delay, frequency response, temperature etc. Parameters are monitored and compared to the expected values under certain circuit operation conditions. Both methods are shown in the Figure 1.3.

IC testing can be either external or internal (embedded). In the early days of IC design, the testing of IC's started as bench-top testing. An external source of input stimuli would be applied to the circuit under test (CUT), and circuit response would be collected and analyzed at the output. This was sufficient, considering the small number of devices per chip and the low speed at which the chips operated. As IC complexity and speed increased, it was more difficult to fully test IC's on the bench. This led to the development of automatic test equipment (ATE). ATE resulted in the integration of a collection of interconnected and synchronized bench-top instruments into a test station.

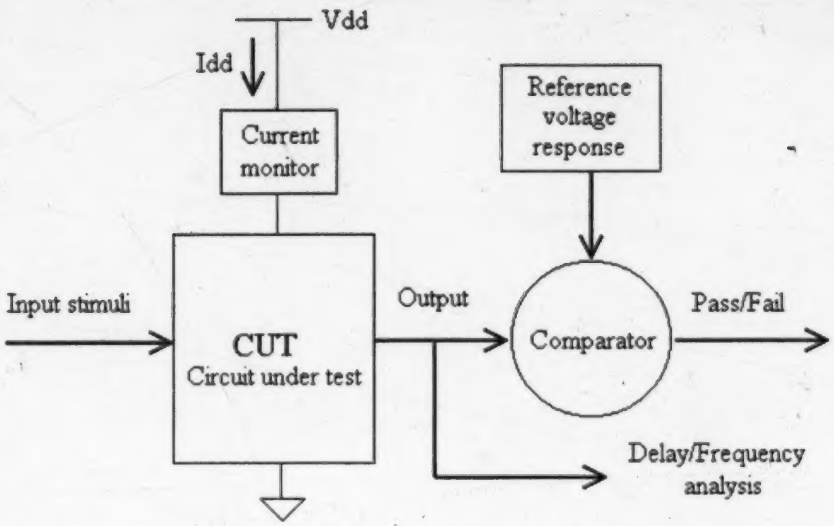

Figure 1.3: General testing environment

The main drawback of ATE equipment is its high cost. With the next generation of IC technology, the testing of even more complex circuits operating at high speed can not rely only on external testing. The idea of internal or embedded type testing was thus introduced. Scan path and built-in-self-test (BIST) designs are the most widely used embedded methodologies. Testing hardware added to the chip performs the function of analyzing and monitoring the operation of the chip. In scan design methodology, specially designed memory elements are used so thet.al.l or some subset of these memory elements can be fully controlled and observed via some special access mechanism usually consisting of one or more shift-register scan-chains. A scheme of the embedded testing is depicted in Figure 1.4. A low-bandwidth signal is generated by the external source and transported to the internal source/sink at the speed at which the signal can be handled bye the I/O's. This high bandwidth signal is processed internally, and the final processing result is handed out to the external source/sink for evaluation. The idea of embedded test hardware was defined as "design for testability". Economic factors favor for embedded testing. The application of embedded testing circuitry reduces the need for expensive ATE.

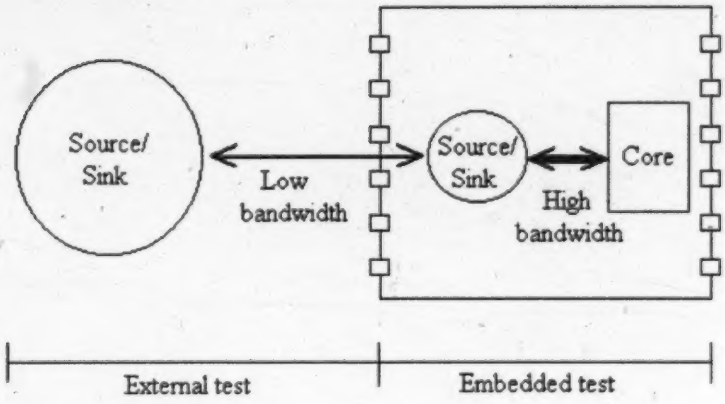

Figure 1.4: Embedded test

Today, the increasing gap between external and internal bandwidth is the main limiting factor in at-speed testing in the application of external testing equipment. The at-speed testing is performed at the rated operational speed of the circuit. As a result of this tendency, it will not be possible to test chips with external testing equipment in the near future. It is predicted that the balance of external and internal testing functions will shift to the solely internal ones. Embedded testing will most likely rise to the higher level of the IC testing, where diagnostics, measurement, debugging and repair will be possible with the next generation of IC designs.

Two basic testing methods are off-line and on-line testing. *Off-line testing* is more traditional and is performed when the normal operation of the circuits under test is interrupted. See Figure 1.5. The circuit enters test mode and is either switched to ATE equipment or tested by the BIST structure. The main drawback is the memory limitation of ATE. Even with medium complex circuits, large amounts of response information have to be stored in order to evaluate circuit performance. Another problem is the long connection lines between the CUT and ATE. These lines can introduce parasitic effects and limit the reliability of the testing. *On-line testing* is performed during the normal operation of a circuit and in a few different modes (Figure 1.5). There is the possibility of concurrent checking, testing in intervals, or testing during the idle operation of the circuit.

When the CUT is in the idle state the user has a higher priority, and testing can be interrupted at any time. A larger part of the testing procedure is performed by the BIST circuitry, so that ATE equipment can be significantly simpler. The area overhead required for the BIST structure is expected to be less than 15% of the CUT.

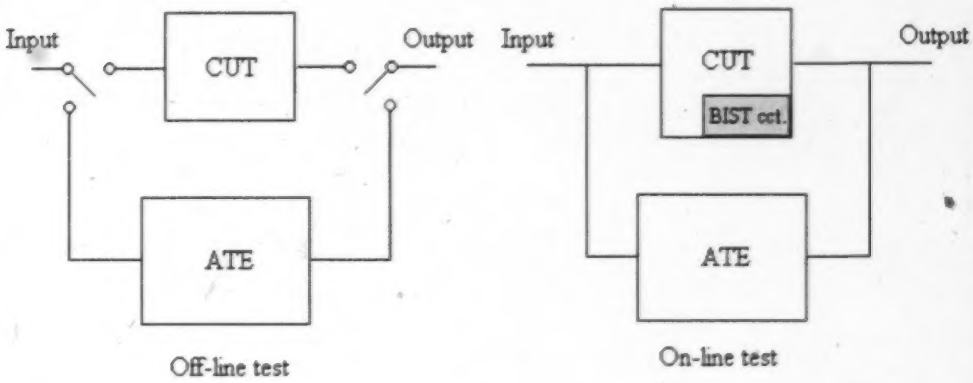

Figure 1.5: Off-line test and on-line test

A number of testing techniques are available today for the testing of very large scale integration (VLSI) circuits. Generally, these techniques can be classified into five different methods:

- *Functional testing:* the CUT is tested in normal operation mode at its rated speed
- *Structural fault testing:* the CUT is tested for permanent faults such as stuck-at-fault, bridging faults, shorts, etc., The circuit can be operated at a lower speed
- *Inductive fault analysis*: a simulation is used in the analysis of the defect generation mechanisms for possible permanent faults. In this case as well, the CUT does not have to be operated at the rated speed.
- *Delay testing:* the CUT is tested at its rated speed and observed for any delays in signal propagation.
- *Current monitoring:* the voltage supply current, drawn by the CUT, is analyzed while different input conditions are applied to the circuit. This can be done either when the circuit is in the static (quiescent) or dynamic (transient) state.

Functional testing is the oldest approach. A sequence of input vectors is generated and fed into the CUT. The advantage of this approach is in the fact that these tests can verify the correct operation of the CUT and that test vectors are already available from test cases used by the design engineer. Even though these tests discover a large percentage of faults, the fault coverage has recently come under question. The major drawback is that even the testing of relatively small digital circuits, such as a 32-bit adder, requires a pattern of 2^{65} input vectors, rendering this approach inapplicable even with the fastest ATE tools.

Structural testing is based on "stuck-at" fault models that are artificial presentation of failures in digital circuits. The stuck-at fault model is the most widely used in IC testing. This fault model is based on the assumption that one of the connection lines between the digital gates is permanently stuck at some logic value, "0" or "1". Stuck-at fault can be single or multiple, if it happens in various parts of the circuit. A single stuck-at fault model is shown in Figure 1.6.

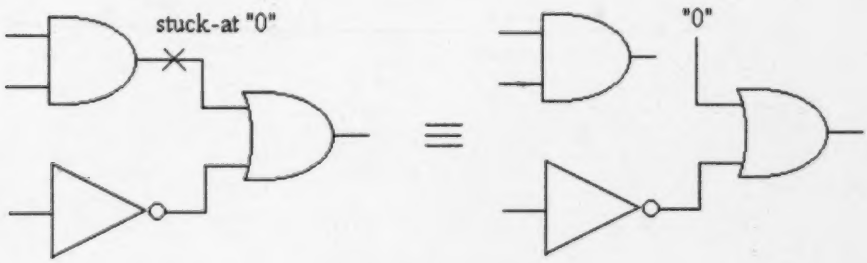

Figure 1.6: Stuck-at fault model

Experience shows that this type of fault modeling can detect a high percentage of faulty IC's. The biggest advantage of this type of fault modeling is that the response of the digital circuit can be mathematically analyzed, using Boolean algebra. The CUT response is analyzed after the previously defined set of test vectors had been applied to the CUT input. There are a number of techniques to define test vectors (*test pattern generation – TPG*), some of which are based on Boolean algebra, some on search-

algorithms, and on a combination of the two previous techniques. An inability to use the stuck-at type model with certain types of CMOS failures has resulted in alternative fault models such as stuck-open, stuck-on and bridging fault models.

Furthermore, limitations of permanent fault models in digital circuits inspired development of alternative approach as to fault modeling, namely *inductive fault analysis* (IFA). By means of simulation, faults resulting from particular modes of failure, such as particle contamination, are inserted into the circuit. These faults can be in the form of metal blobs causing shorts between two interconnection lines or some other deviations on particular layers of the IC. The main advantage of IFA is that modeled faults are more realistic as compared to the traditional stuck-at fault models. The main drawback is that the technique is time and cost extensive, since it requires sophisticated testing equipment.

Delay testing is based on the assumption that these delay-type of faults do not affect circuit performance, but circuit functionality. This means that a circuit will operate correctly at a low speed but will fail at the rated speed. Two types of delay models are the gate delay model and the path delay model. The former assumes a delay at a certain gate; the latter one assumes a delay accumulated along the path of signal propagation. The disadvantage of delay testing is that it is very sensitive to additional delays in other parts of the circuits that are not the target of the testing.

In current monitoring, the voltage supply current drawn by the circuit under test is monitored and compared to the reference current value. It is assumed that a faulty circuit produces an abnormal or at least a significantly different amount of current compared to the current produced by fault-free circuits. There are two types of current monitoring: quiescent current monitoring--Iddq, performed after the input has been applied and the CUT has reached its stable (quiescent) state and transient current monitoring--Iddt, the monitoring of the dynamic current at the time of input application. Monitoring can be done externally using ATE or internally using built-in-current-sensor (BICS). Traditional voltage-based testing techniques, such as stuck-at-fault, have limitations in detecting faults that do not affect output voltage levels such as shorts and bridging faults. Also, certain faults cannot be described by the stuck-at-fault model and show the necessity for more realistic fault modeling. In both cases, current monitoring has proved to be very effective in the detection of these faults and it is widely used in the industry, mostly as

Iddq testing. The major drawback of this type of testing is the degradation of CUT performance as a result of the insertion of a current sensing element into the current path between the CUT and the ground between the CUT and the voltage supply. The largest obstacle for Iddq is its low testing speed. Since a quiescent current can be observed only after the transient part has settled down, a high testing speed cannot be achieved. A few recent papers argue about the limits that Idqq testing has reached. The increased complexity of VLSI circuits with a high density of devices on the same chip has resulted in high levels of static current and the problem of setting the quiescent current reference value. In any case, Iddq testing currently provides valuable tool in the detection of shorts and bridging faults, and Iddt continues to be an attractive research subject.

1.4 Thesis Summary

Limitations in traditional stuck-at fault testing methodologies show necessity for more efficient testing approaches. As well, faults that cannot be modeled by existing fault models require the development of a new testing methodologies. A current monitoring technique demonstrated the potentials in overcoming these obstacles in VLSI testing. Additionally, built-in current monitors provide the possibility for on-line testing, performed during the normal at-speed operation of the CUT. These were the main reasons for the selection of current monitors, as a subject of the research presented in the thesis.

The thesis presents two designs of built-in current monitors for on-line testing VLSI circuits. Both monitors are designed in low-voltage environment. The first design is the improved version of the Stopjaková/Manhaeve design, described in Section 2.6.3. The second monitor is the new design based on the unbalanced current mirror design. This design introduces additional sensing element which improves sensibility of the current monitor.

Current monitoring is the subject of this thesis and it is described in greater detail in the following Chapter 1. Chapter 2 provides background information and literature review. Definitions of the quiescent and the transient current monitoring are presented.

Various designs of current monitors are discussed along with examples of each of the analyzed approaches. Previous work is discussed with comments on every given example.

Chapter 3 proposes an improved design of current monitor based on earlier designs. The monitor is designed for the testing of Low-Voltage environment (1.5 V) circuits. The design is then implemented in 0.35 μm and 0.5 μm technology and. It is intended for monitoring both quiescent and transient current elements. The design is suited for the testing of digital circuits. Simulation results are discussed and analyzed. Finally, measurement results of chips implemented in 0.35 μm and 0.5μm are provided.

Chapter 4 presents a new current monitor for combined Iddq and Iddt testing. This is also a low-voltage design that can be applied to mixed signal (analog/digital) circuits. Its design is simulated and manufactured in 0.35 μm and 0.5 μm technology. Simulation and measurement results are discussed.

Chapter 5 gives an overview of future developments in the field of current monitoring. A new idea for introducing an inductive element as a sensing device is elaborated. A new design of the solenoidal inductor is proposed.

Chapter 6 draws conclusions about the work described in the thesis and summarizes the presented material.

Chapter 2

Background and Literature Review

This chapter presents background and literature review on current monitoring. Current behavior of CMOS circuits is presented in the Section 2.1. Section 2.2 contains a description of the fault models used in testing by voltage supply current. Section 2.3 defines the basics of current monitoring, including Iddq and Iddt monitoring techniques. Limitations of current monitoring are explained in Section 2.4. In Section 2.5, various aspects of technology scaling are described. Design of current monitors, presented in a literature review, is given in Section 2.6.

2.1 Current Behavior of CMOS Circuits

Two elements of the voltage supply current Iddq – quiescent current and Iddt – transient current can be seen in Figure 2.1. During the switching phase of the CMOS circuit, a dynamic (transient) current is drawn by the circuit. After the settling period, when the CUT has reached its stable state, current drawn by the CUT becomes very small, and it is referred to as leakage or quiescent current.

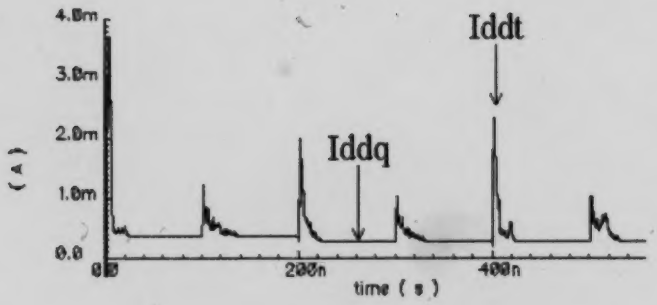

Figure 2.1: Voltage supply current (Idd)

2.1.1 Quiescent Current - Iddq

Quiescent or Iddq current is made of two major components: the junction leakage current and subthreshold leakage current [5]. Both components can be seen in Figure 2.2.

Junction Leakage Current

Reversed biased PN-junction leakage currents result from various mechanisms such as diffusion and thermal generation in the depletion region of the PN-junctions [6,7]. The leakage currents of reverse-biased sources and drain junctions are state-dependent, while the leakage current of reverse-biased well-substrate junctions is state-independent (Figure 2.2). A simple model that describes formation of parasitic PN-junctions for a CMOS inverter will help understand the mechanism of leakage involved in the device (Figure 2.3). The source-drain diffusions and the n-well diffusion form parasitic diodes. As well, one diode is formed between the substrate and the n-well.

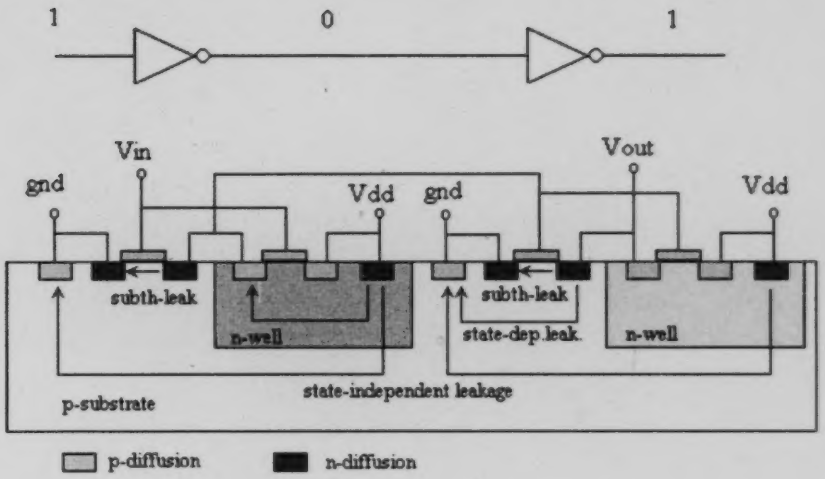

Figure 2.2: Junction leakage current and subthreshold current

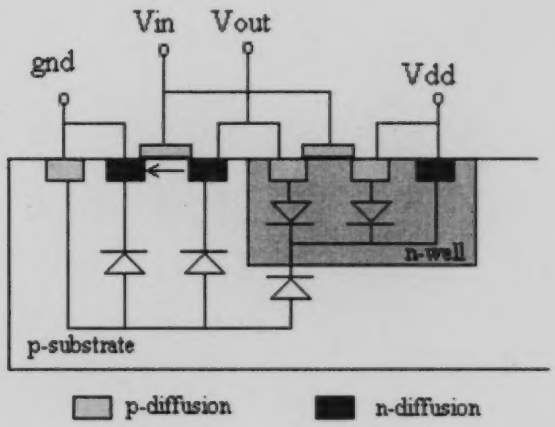

Figure 2.3: Parasitic PN-junctions in a MOS device with a p-substrate

Junction leakage currents can be estimated by the formula:

$$I_{leak} = Js\sum[Ai] \tag{2.1}$$

where Js is the reverse saturation current density of the PN junction defined by the process, N is total number of reverse-biased PN junctions and Ai and the total area of the i-th junction. The total area A can be estimated as:

$$A = W \cdot L \cdot \pi \cdot X_j \cdot (W + L) + \frac{\pi}{6} X_j^2 \tag{2.2}$$

where W and L are the width and the length of the device and Xj is the junction depth. For simplicity, Figure 2.3 describes junction areas as rectangular, but in reality, there is always some roundness in diffusion areas. To include this curvature-effect, the π multiplier was introduced in Formulas (2.2) and (2.3). For a well-substrate PN junction, the effective area A is estimated by equation (2.3):

$$A = W \cdot L \cdot 1.6 X_j \cdot (W + L) + 0.8\pi \cdot (W + L) + \frac{\pi}{6}(0.8 X_j)^2 \tag{2.3}$$

Subthreshold Current

Subthreshold current is generated when the gate voltage is lower than the threshold voltage Vt and there is some voltage between the source and drain of the MOS transistor [8]. It is generated by the minority carriers and diffusion. The carriers move in a similar way as they would move in the base of a bipolar transistor. This component is state independent. Subthreshold current depends exponentially on Vgs and Vds through the carrier concentration. The subthreshold current in an NMOS transistor can be estimated by the following equation:

$$Ids = \mu_N Cox \frac{W}{L} V_t^2 \exp\left[\frac{Vgs - V_{THN}}{nV_t}\right] \times \left(1 - \exp\left[-\frac{Vds}{V_t}\right]\right), \tag{2.4}$$

where μ_n is the electron mobility, Cox is the gate capacitance by the area, W and L are length and width of the device, Vth is threshold voltage and V_T is the thermal voltage.

Other leakage currents may appear in CMOS technology, but these currents are undesirable and here are assumed to make up a small portion of the total leakage current:

- Gate-induced drain leakage currents: it occurs with the low gate and high drain bias due to band-to-band tunneling of electrons across the pn-junction in the gate-to-drain overlap region where a high negative electric field exists in the oxide [9]. These currents flow from drain to substrate.

- Bulk punch-through current: It flows from the drain to the source due to a lateral bipolar transistor formed by the source (emitter), the bulk (base) and the drain (collector).This component is controlled by raising the impurity concentration in the bulk channel region.

- Tunneling currents: These are generated across the oxide between the gate and drain. For feature sizes above 0.1 μm, they are assumed to be negligible [10].

2.1.2 Transient Current - Iddt

The peak of Iddt can be estimated by taking into account the number of switching nodes at the time of evaluation [11]. Drive strength and capacitance of switching nodes determine this peak value of the supply current. Quantification of these elements is possible through the electrical models and the parameters characteristic of the technology in use. The estimated transient current is:

$$I_{TRmean} = \frac{1}{T_{TR}}\left(Vdd \cdot \sum_{H}^{L} C_i + \sum I_{SCj} + \sum n_k \cdot I_{FTk} \right) \qquad (2.5)$$

where T_{TR} is switching period, Vdd—power supply, Ci—node capacitance, n_i—circuit node. The main contributor to I_{TR} is capacitance charging currents, the first term. The

second term in equation (2.5) is the short circuit current at the switching nodes. The last term is the stochastic current representing the contribution of false transitions that may depend on circuit design, input pattern and signal timing.

If N--the number of switching transistors is very large, like in case of VLSI circuits, then the transient peaks value can be very high. This high value of the current peaks presents the main problem in the design of current monitors. To be effective, current monitors must have, on one hand, a very large dynamic range for these high transients, and on the other hand, they have to be very sensitive and have high resolution in order to detect low values of leakage currents. Consequently, dynamic current monitoring has not yet found practical implementation in industry. Two exactly opposite requirements, a small impact on the circuit under test and high sensitivity for the wide range of voltage supply currents, render design of dynamic current monitors extremely challenging.

2.2 Fault Modeling

In the presence of a fault, current response of the CUT depends on the type of the fault involved. Short and bridging faults result in increased levels of static and dynamic current being drawn by the CUT, whereas open faults lead to decreased activity of the CUT, reducing the Iddq and the Iddt values. Fully understanding the mechanism of faults and the behavior of voltage supply current in the presence of fault requires a proper understanding of fault models. Most physical defects can be classified as "shorts" and "opens". The fault models involved in MOS are electrical models of defects such as gate-oxide shorts, bridging faults, floating gates and open faults. These models are used in simulation analysis in order to obtain results of the specific failures and their impact on circuit performance.

2.2.1 Shorts

These faults result from unintended connections between metal, polysilicon or conducting paths through insulation layers. The s-a-f test is not always able to detect these faults. However, most shorts will produce an abnormal current that can be easily detected. Shorts of particular interest in the testing of CMOS circuits are gate-oxide shorts (GOS) [12], electrical connection through the thin oxide between the gate and the silicon surface of a MOS transistor (Figure 2.4).

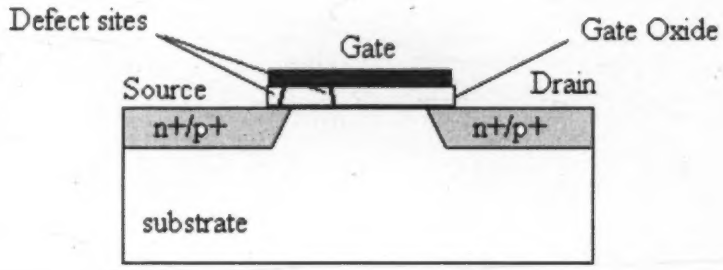

Figure 2.4: Structure of gate-oxide short in a MOS-transistor

GOS result from the manufacturing process or material defects. All shorts located in the gate-source region and gate-drain region can be classified as one type of shorts. The second type of shorts is located in the channel region, far away from the gate-source and gate-drain area. The structure and models of NMOS and PMOS models of gate-oxide shorts are illustrated by Figure 2.5 and Figure 2.6. These shorts are very hard to detect, and testing of VLSI circuits presents special problems [13]. Gate-oxide shorts cause the Idd current to increase, and in most cases, logic voltage levels and propagation delay times to degrade. However, the functionality of the circuit may not be affected by the GOS.

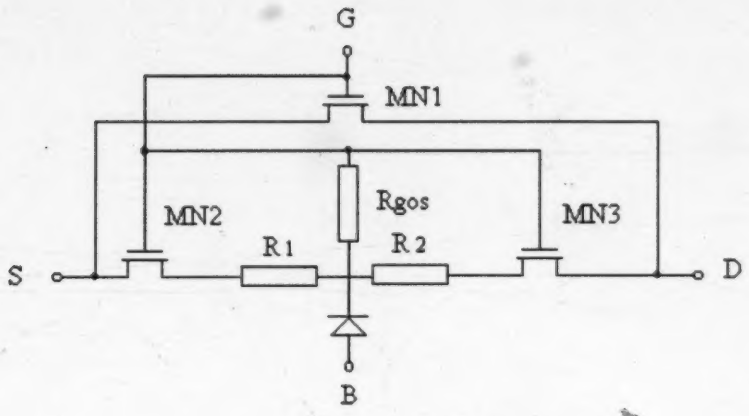

Figure 2.5: GOS model for NMOS transistor

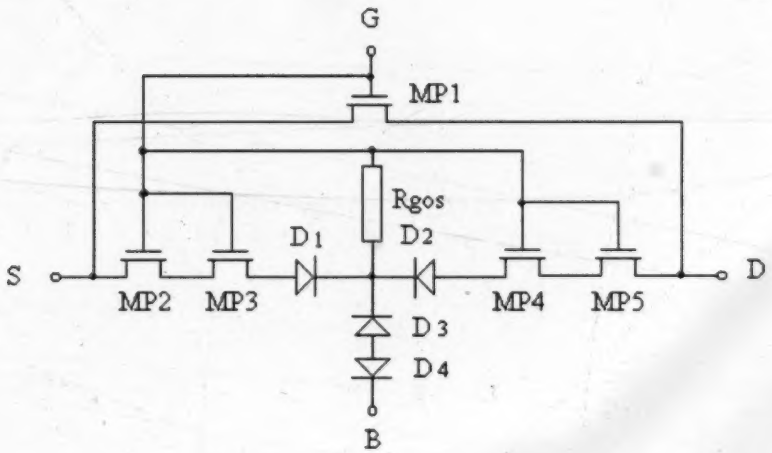

Figure 2.6: GOS model for PMOS transistor

2.2.2 Bridging Faults

Bridging faults occurs when two or more conducting lines are interconnected or when the insulating material is missing . These faults may originate during the fabrication of in field-operation. These defects are classified as horizontal bridging interconnections inside

the same layer or as vertical bridging interconnections between different layers. Figure 2.7 shows the fault model of the bridging defect. A bridging fault in a MOS transistor can result in bridging between any two of transistor's four terminals. Since it does not behave as a permanent stuck node to a logic value, the bridging fault typically cannot be modeled as a stuck-at-fault model. A bridging fault can be represented by the resistor connecting two interconnection lines or layers (Figure 2.7).

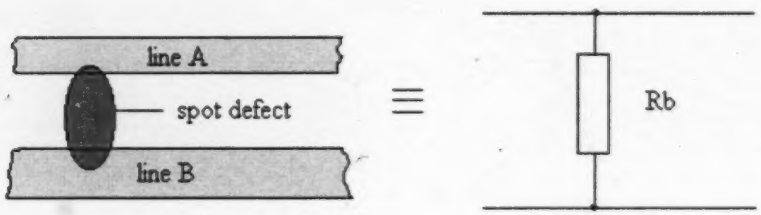

Figure 2.7: Bridging fault model

These faults can be divided into high-resistance and low-resistance faults. Statistically, most low-resistance bridges occur between two conducting layers and have a value below 500 Ω [14]. In this case, they cannot be ignored like high-resistance bridges. Bridging faults usually lead to propagation delay times. Hard bridges cause degradation of voltage levels, stuck-open and stuck-on faults.

2.2.3 Open Faults

Open faults appear when the conducting path is broken. A conducting path in one of several layers can be broken horizontally or vertically. A break on the gate connection results in a floating gate. Another important fault is source/drain open. The floating gate fault model is presented in Figure 2.8. C_{PM} represents capacitance poly-metal and C_{PB} represents poly-base capacitance.

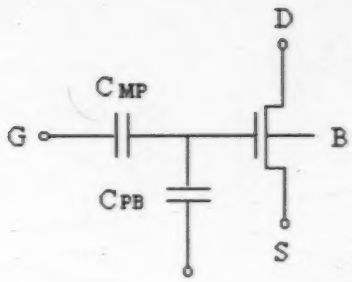

Figure 2.8: The Floating gate fault model

2.3 Current Monitoring

More than a decade ago, supply current monitoring was introduced as a very promising method in the testing of CMOS circuits. This method is based on the fact that defective circuits produce an abnormal or at least significantly different amount of current compared to the current produced by fault-free circuits. This excess current can be sensed and fault detected.

The power supply current (Idd) can be defined by its two elements: Iddq--quiescent current and Iddt--transient or dynamic current. Iddq is basically a leakage current drawn by the CMOS circuit when it is in its stable (quiescent) state. Iddq testing relies on the fact that defect-free CMOS devices have a very low leakage current when the circuit is in the quiescent state. For Iddq testing to be successful, it is important that defective current be significantly higher than the fault free current value. A general distribution of Iddq values in a CMOS network is presented in Figure 2.9, where Mg and Md represent the mean values for non-faulty and faulty Iddq values, respectively. The decision between faulty and non-faulty Iddq response can be made by setting the reference value between the two distributions.

In order to detect the fault by Iddq testing, the faulty-current path between a power-supply and a ground has to be acitvated. Therefore, a set of CUT's test vectors that will satisfy this condition has to be defined. Iddt is a supply current produced by the circuit under test (CUT) during the transition period after an input has been applied to the CUT. Every input vector produces different dynamic-current response of the CUT. If

there is an active fault, circuit's current response will differ from the normal current response. This information about the CUT is used in the Iddt testing.

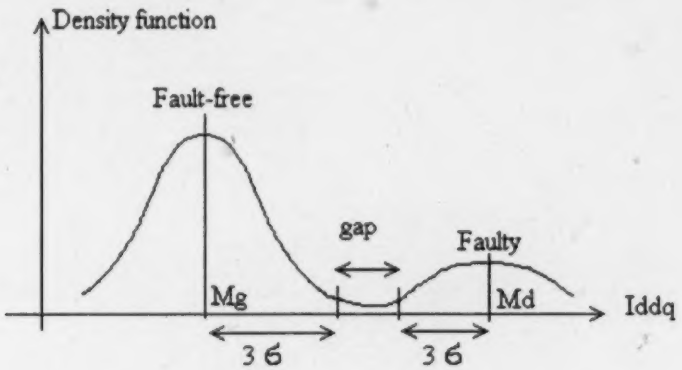

Figure 2.9: General distribution of the Iddq values in CMOS network

Numerous current monitoring techniques as well as numerous designs of current monitors have been proposed. Most of these are Iddq-based techniques. Iddt testing has not yet found practical implementation in industry because of the difficulty of extracting of useful information from fast-changing current response. Current pulses can range from several μA's to a few hundred of mA's. Even though only Iddq techniques have been used in practice, it has been proven that some faults, such as opens, do not affect quiescent current and cannot be detected through this testing. On the other hand, these types of faults affect transient response of the circuit and can be detected by Iddt testing. Consequently, Iddt can be used as a powerful complementary technique.

Some researches argue that Iddq testing has reached its limits as a result of device scaling [15]. This is supported by predictions of the Semiconductor Industry Association's (SIA) road map for the next fifteen years of development of submicron technologies (The National Technology road map for the Semiconductor Industry Association 1994). On one hand, SIA objectives encourage further work in Iddq testing because Iddq testing is very efficient in detecting faults resulting from decreasing device sizes and from increasing circuit complexities [16]. On the other hand, the SIA road map

questions the efficiency of Iddq testing because of a radical increase of leakage current in high-density integrated circuits.

One of the parameters that has been affected by scaling is leakage current. A critical requirement of Iddq testing is accurate measurement of a very small current. Typically, the Iddq threshold for the decision pass/fail making is set to 1 μA to 10 μA. In order to make a correct decision, the Iddq of a fault-free CUT has to be at least one order of magnitude lower than the Iddq threshold. With millions of devices on a single chip, leakage current becomes significant. As a result of increased current leakage, the values of fault-free and faulty Iddq current start to overlap, and it is impossible to set an adequate threshold value. Partitioning of the CUT into smaller parts which lowers leakage current to some acceptable level, is one way of overcoming this problem [17].

2.3.1 Current Monitoring Methodologies

Several different methodologies have been developed to test VLSI CMOS circuits. Classification can be done by the type of the circuits being tested or by the specific approach used in the monitoring technique. Also, as mentioned in the previous chapter, current monitoring can be done externally or internally by built-in current sensor, as well as off-line when the circuit is not in the normal mode operation and on-line when the operation of the circuit is not interrupted.

Depending on the type of circuit being tested, different methods for digital and analog/mixed-signal circuits exist. Depending on the approach, CUT current response can be analyzed using reference voltage analysis, signature analysis, waveform analysis, etc.

Monitoring of Digital Circuits

The traditional technique for testing digital CMOS circuits is voltage testing by using stuck-at-fault modeling. As was mentioned in the previous section, a number of failures cannot be modeled by the stuck-at fault model. Moreover, certain types of CMOS faults, such as gate-oxide shorts, certain bridging faults, certain open faults, stuck-on faults, punch-through faults, operation-induced faults and soft pn-junction faults, may not

manifest themselves as logic faults. Parametric faults such as incorrect threshold voltages, excessive parasitics, etc., are also difficult to detect by the traditional voltage techniques but often affect signal time propagation delays as well as power consumption of the circuit. Iddq monitoring techniques have shown to be very effective in detection of these types of faults. Iddq tests implemented prior to the burn-out test can significantly decrease fall-out.

In functional testing, the site of the fault has to be excited and the effect of the fault has to be propagated to the output. In current monitoring, testing the propagation of the fault is automatic. The current response is picked up by the current monitor and compared to the reference value. The scheme for current monitoring is shown in Figure 2. 10.

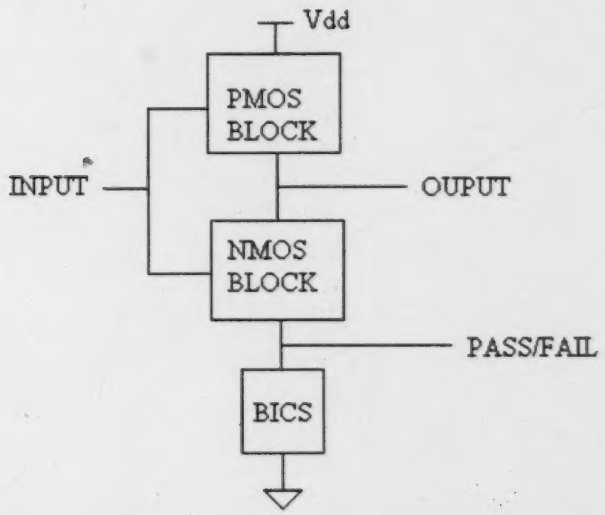

Figure 2. 10: Current monitoring scheme for CMOS digital circuits

Monitoring of Mixed-signal Circuits

In recent years, the success of current monitoring in testing VLSI digital circuits has inspired researchers to try to implement current monitoring technique in testing of mixed-signal integrated circuits (MSIC). As well, the implementation of digital and analog devices on a single chip has supported the great need for the development of reliable testing techniques for this type of circuit. Nevertheless, testing of mixed-signal circuits presents far more complex problem than testing of digital circuits. Analog circuits are characterized by many parameters including gain, frequency, phase shift, etc.; therefore proper operation of a CUT, including monitoring of all parameters, is not an easy task.

Many techniques have been proposed for testing MSIC circuits. Many of them use the division of a circuit on a digital and an analog part, where tests are applied to each part separately. The problem with this approach is that analog parts contain circuits such as A/D converters and switched-capacitor circuits that exhibit characteristics of both analog and digital circuits. Several papers discussing the implementation of current monitoring techniques apply only transient current analysis [2,3] or integration of current signal. [1]. The first technique does not consider the quiescent response of the CUT and the second one can result in a high level of aliasing, that is, in a number of identical responses as a result of current averaging.

Time-Domain Analysis

A procedure for testing of mixed-signal integrated circuits (MSIC's), called "time-domain testing," was used in the work for this thesis [2]. The basic idea is explained in Figure 2.11.

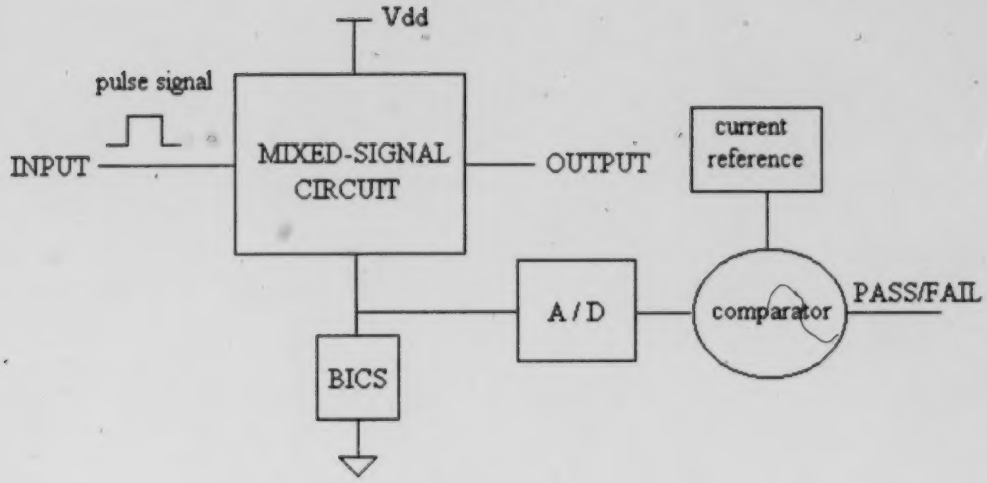

Figure 2. 11: Time-domain analysis for mixed-signal circuits

This procedure is based on the excitation of CUT with a series of pulses at the same time that the current response is monitored and evaluated. This response is digitized and compared to a predetermined fault-free value. This predetermined value represents signature of the CUT. Of course, this value depends on the input value, so changing the input stimulus produces different signatures for static states-- state-high and state-low and transient states--low-to-high and high-to-low.

2.4 Limitations of Current Monitoring

Testing of integrated circuits by current monitoring has some limitations. These are due to the fact that in order to detect a fault in an IC, a fault has to be activated by activating the current path through the fault. In certain circuit configurations, when this current path cannot be activated, the fault cannot be detected. Also, with constant scaling of device sizes with new technologies together with increased density of integrated circuits, leakage currents have increased to the level where it is not possible to set a reference value between the normal and the faulty current value.

2.4.1 Limitations in Detection of Shorts

Shorts are faults resulting from unintended connections between metal, polysilicon or conducting paths through the insulation layer. The s-a-f test is not always able to detect these faults. However, most shorts will produce an abnormal current, which can be easily detected. An excessive amount of current will be produced if an input pattern can connect the VDD node to the GND node. If we consider a short between nodes (1) and (2) in Figure 2.12 and apply a logic "high" to A and B, VDD and GND will be shorted, and excessive Iddq will be registered, and a fault will be detected. Figure 2.13 shows limitations of the Iddq method [1]. If we consider a short between nodes (1) and (2), both nodes will be charged to VDD or discharged to GND when the clock is "high." In this case both nodes are at the same potential, so it will not result in a significant Iddq current, and the fault will not be detected.

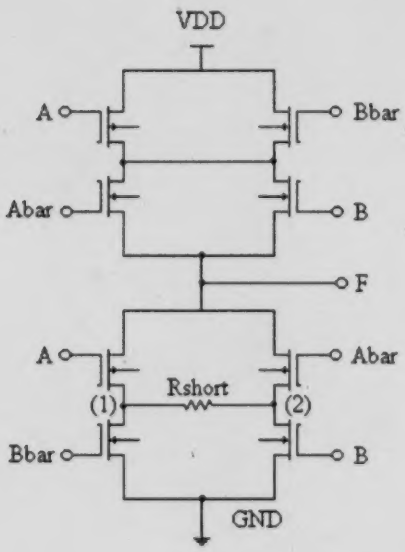

Figure 2. 12: Limitations of s-a-f test

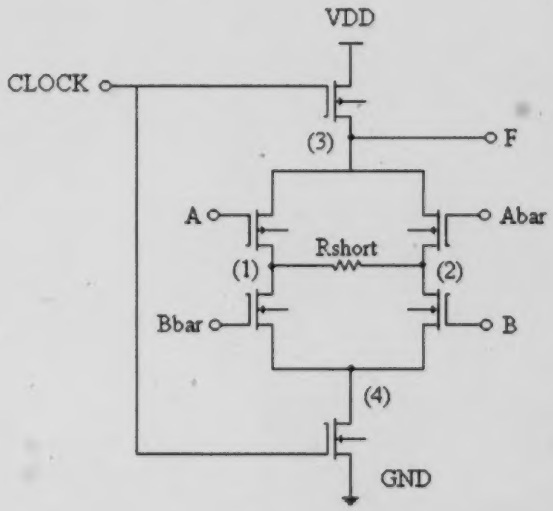

Figure 2. 13: Limitations of I_{DDQ} test

2.4.2 Limitations in Detection of Open Defects

Open defects happen when a conducting path in one of several layers can be broken horizontally or vertically. The two most important open defects are floating gate and source/drain open.

The Iddq test may not always detect an open defect. Figure 2.14 shows a source/drain open defect (node 3). If transistors T1 and T3 or T2 and T4 are on, and the clock input signal goes from "high" to "low" or "low" to "high", a temporary path from PWR to GND induces a high Iddqt peak. However, this path will be removed because of the source/drain open, and the Iddq will not detect the fault.

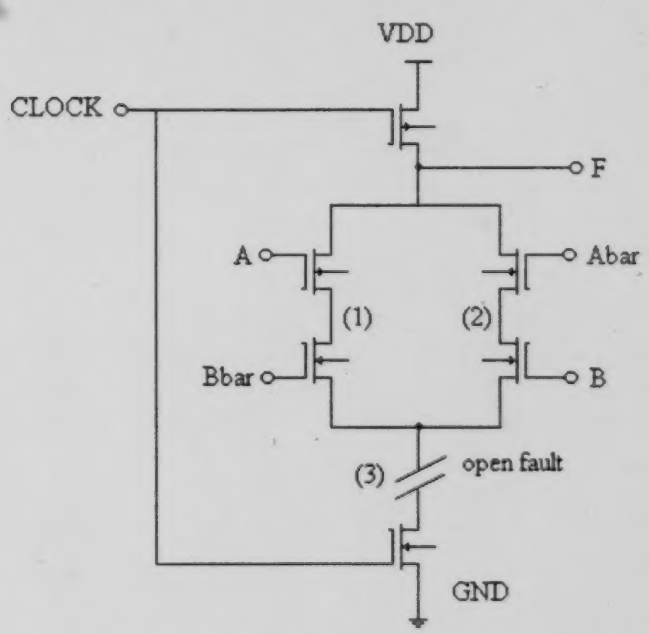

Figure 2.14: Source/drain open

These examples as many other experiments demonstrate that the s-a-f test and the Iddq test cannot always detect these faults, whereas the Iddt test is able to do so. The comparison of these three techniques' statistical data for the overall defect coverage is shown in Table 2.1. Two hardware experiments are conducted by Shyang et.al. [17]. Both experiments include IC designs with built-in defects and physical measurements of both, power supply current response and output voltage response. Four types of faults were observed: open drain/source, single floating gate, double floating date and short in the pre-charge chip. Experimental results of the fault coverage are very encouraging and show high fault coverage in case of Iddq and Iddt test methods.

Table 2.1: Overall defect coverage data

	DEFECT COVERAGE (%)				
	Total gates tested	Iddq	Iddt	Iddq+Iddt	Logic test
Open drain/source	128	28.1	96.9	100	72.7
Single floating gate	56	92.9	100	100	64.3
Double floating gate	44	90.9	100	100	90.6
Short in pre-charge	8	0.0	100	100	100

2.5 Aspects of Technology Scaling

The basic idea of scaling, shown in Figure 2.15, is to reduce the dimensions of the MOS transistors and the wires connecting them. The scaling of devices affects numerous device parameters, one being the subthreshold currents or leakage current [18]. Plotting the distribution of the Iddq values for a collection of chips from the same CMOS network should reveal a bimodal distribution, similar to the one shown in Figure 2.9. The first normal segment of the distribution depicts the Iddq values in the non-defective

device, with a mean value denoted by Mg. The defective parts drawing excessive current due to the presence of a defect have their own distribution with higher values for the quiescent current, with the mean value Md. If the two distributions are far apart, a quiescent current limit can be selected that differentiates the non-defective product from the defective one. As long this separation gives an discriminatory difference, testing can be sufficiently reliable.

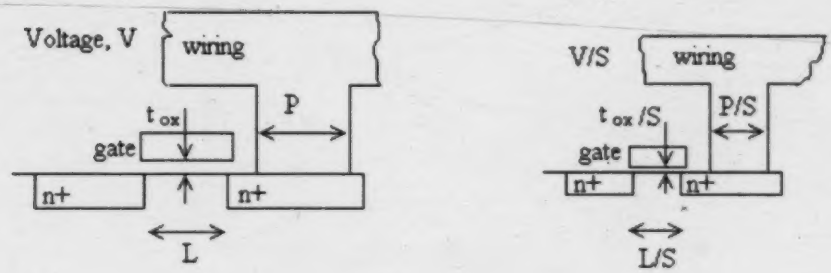

Figure 2.15: Device before and after scaling

Iddq is basically the leakage current in a CMOS when it is in a stable state. This leakage occurs when the transistor is in a cut-off region where the drain-source current can be approximated with formula (2.4) which is repeated here for the convenience:

$$Ids = \mu_n Cox \frac{W}{L} V_T^{\,2} \exp\left[\frac{Vgs - V_{tn}}{nV_T}\right] \times \left(1 - \exp\left[-\frac{Vds}{V_T}\right]\right) \qquad (2.6)$$

[μ_N- surface mobility of carriers, Cox-gate oxide capacitance, Vtn-threshold voltage, V_T-thermal voltage, W- gate width, L-gate length].

In the low-voltage/low-power design, reducing the channel length also reduces the peak of the surface potential and increases the current [4]. If Vdd is reduced, the peak is further reduced. Therefore, the short channel effect contributed to the penetration of the junction electric fields into the channel region, causing a lowering of the barrier and V_{th} reduction

leading to further increasing of the leakage current. The low-voltage/low-power circuits can be mainly designed by two techniques: constant field scaling and reducing the Vdd.

2.5.1. Constant Field Scaling

The scaled design is obtained by applying a dimensionless factor S to all dimensions including those vertical to the surface, device voltage and the concentration densities. As a result, V_{th} is reduced by factor α and the gate-oxide capacitance given in the equation (2.7) also decreases by the same factor.

$$C_{ox} = \frac{\varepsilon WL}{t_{ox}} \tag{2.7}$$

Therefore, Ids is reduced. If we define I_f as the faulty current drawn by the CUT, the I_f will also decrease by the factor S: $I_f' = I_f/S$. Since the fault-free current is increased, and the faulty current is decreased, the ratio between these two currents is therefore reduced. As a result, distinguishing faulty from the fault-free current value is diffucult.

2.5.2 Reducing supply voltage Vdd only

By decreasing the supply voltage Vdd, drain-source voltage is reduced. According to formula (2.8) V_{th} will increase:

$$V_t (Vds) = V_t^* - \sigma Vds \tag{2.8}$$

[V_t^* - threshold voltage at low Vds < 0.1 V, σ - drain induced barrier lowering parameter]

Therefore, the leakage current will also decrease. As a result, the faulty and the fault-free values decrease, the ratio is preserved, and in this case, the Iddq test methods can still be used in this kind of low power circuits.

The impact of changing design and operating parameters on the effectiveness of Iddq testing can be analyzed by calculating the distance between the two means Mg and Md of the distribution, according to equation (2.9)

$$\frac{Md - Mg}{Mg} \qquad (2.9)$$

Technological trends used on analysis are shown in Tables 2.2 and 2.3 [15]. The Ioff is the subthreshold current estimated over limited interval of device parameters and at zero gate voltage.

Table 2.2: Trends in CMOS technology at 100°C (SIA roadmap values)

Year	Gates ($x10^6$)	Vdd(V)	Leff (um)	Max I_{dd}off (nA/μA)
1995	5	3.3-2.5	0.25-0.45	5-10
1998	14	2.5-1.8	0.21-0.25	10-20
2001	26	1.8-1.5	0.1-0.15	20
2004	50	1.5-1.2	0.1-0.15	30
2007	210	< 1.2	< 0.1	30

The fifth column of the Table 2.2 shows estimates for the Max Idd_{off} at 100°C as given in the SIA Roadmap [1]. The fifth column in Table 2.3 is the more accurate estimate, according to the [1], assuming that V_t is scaled down directly with the Vdd.

Table 2.3: Trends in CMOS technology with scaling V_t proportional to Vdd at 25°C.

Year	Gates ($x10^6$)	Vdd(V)	Leff (um)	Average Idd_{off}(nA/μA)
1995	5	3.3	0.45	0.004
1998	14	2.5	0.25	0.12
2001	26	1.8	0.15	2.5
2004	50	1.5	0.10	14.2
2007	210	1.2	0.07	82

The calculation of Mg and Md are based on several assumptions. If the calculation is based on Max Idd_{off}, then it is assumed that only 10% of all the gates in the network would have Idd_{off} values near the maximum of the distribution. The cumulative Iddq current of this 10% of the gates dominates the Iddq value of the good network. If the calculation is based on Average Idd_{off}, all gates in the network contribute towards Mg. Here, it is assumed that only one leaky transistor per gate is present even though there are other possibilities. A defect can cause a gate to have a path from Vdd to GND through one PFET and two NFETs. Assume also that resistance PFETon = 15 k and NFETon = 6 k. Calculations are done by the equations (2.10), (2.11) and (2.12). First, Ioff values from Table 2.2 and Table 2.3 are multiplied by W to obtain Ioff values for a single device.

$$W = 20\ Leff \tag{2.10}$$

$$Mg = Gates\ X\ (10/100) / Max\ I_{dd}off \tag{2.11}$$

$$Md - Mg = Vdd / (2R_{NFET} + 2R_{PFET}) \tag{2.12}$$

Table 2.4 presents the results of the calculation, revealing the sensitivity of Idd_{off} current to the variations of V_t. Table 2.4 demonstrates that ratios of 1/6 or above are required for Iddq testing to be useful. Unfortunately, an increase from 1/10 to 1/6 in Vt/ Vdd will result in about a 20% penalty in speed performance. In today's marketplace, manufacturers are unlikely to be willing to tolerate such an overhead for the benefits derived from Iddq testing. The suggested solution to this problem is the partitioning of the original design. Partitioning created lower Idd current in each portion. This increases the I_{DDQ} observability and improves reliability of the Iddq testing.

Table 2.4: Variation of relative distances (Mg-Md) on ratio V_t/Vdd

V_t / Vdd	Ave Idd_{off} (estim.)	(Md-Mg)/ Mg
1/6	9.9 x 10-4	2670%
1/8	0.02	133%
1/10	0.12	22%
1/20	4.38	0.6%

A similar calculation to that used in an earlier section can be used to determine relative distance between means Md and Mg for the next ten years, using Table 2.3 and Table 2.4. The results are given in Table 2.5.

Table 2.5: Relative distance between the means Md and Mg.

Year	Roadmap (Md-Mg)/Mg	Estimated (Md-Mg)/Mg
1995	19.6%	1358%
1998	3.15%	22.1%
2001	1.28%	0.68%
2004	0.37%	0.08%
2007	0.07%	0.00%

Table 2.5 indicates that Iddq testing will cease to be possible for high performance designs as a device's geometry and power supply voltages are scaled down. In that case, new techniques to control the quiescent current must be developed.

2.6 Current Monitors

2.6.1 Off-Chip and On-Chip Current Monitors

Current-measurement devices can be designed as Off-chip monitors (OCM) and On-chip monitors (Built-In-Current-Sensors-BICS). Both can be classified according to a method using current monitoring. The direct method compares the monitored value to some reference value, and the indirect method uses the conversion of current value to a different quantity such as the voltage drop or the time required for the capacitor discharge [19]. According to the type of sensing element, monitors can be classified as capacitor sensors, resistor sensors or transistor sensors. Nonlinear devices (transistor, diode) can have a better dynamic range compared to linear elements (resistors).

Since OCM is usually implemented by external Automatic Test Equipment (ATE), using BICS has some advantages over the ATE. BICS significantly reduces the test equipment cost. Because of the high capacitance of I / O pads, the testing rate can be significantly reduced. BICS has improved detectability and observability of the circuit-under-test and higher resolution and higher testing resolution. Recently much work has been done in order to improve BICS sensitivity and reduction of the degradation of CUT performance, as these are two crucial elements of the design of a good current sensor.

2.6.2 Design of a Built-In Current Monitors

Built-in current monitors should have the following characteristics [14]:

- High functional speed
- High current resolution
- Small voltage drop due to the testing circuit
- Simple testing circuit
- Small chip area of the testing circuit
- Small performance degradation of the CUT due to the testing circuit

The design of a current monitor is a trade-off between circuit speed, size, sensitivity, and accuracy. The higher resistance of the sensing element leads to an increased sensitivity but also to a lower speed and a higher voltage supply degradation, which is very important for low-voltage designs. A number of current monitors have been built, and a short analysis of some of them follows.

Most of the current monitors presented in the literature use a resistor or a MOS transistor biased in a triode region as a sensing element [20, 21]. The sensing element is inserted into the supply current path, and the voltage drop across the element or the current is sensed and evaluated. When a MOS transistor is used as a sensing element, nonlinear resistive elements are inserted into the Idd path, resulting in a degradation of the performance of the CUT, i.e., additional delay and voltage supply degradation. If a minimum supply voltage degradation and a high testing speed are to be achieved, the size of the transistor needs to be dramatically increased in order to decrease the resistance. On the other hand, a larger parasitic capacitance is achieved with the increased transistor size. Because of this RC parasitic effect, resistor as a sensing element is a better choice for high-speed applications [22].

2.6.3 Previous Designs of Current Monitors

Flip-flop based design proposed by Maly et.al.

This current monitor consists of a flip-flop and a transistor-based nonlinear resistance circuit breaker [23] (Figure 2.16). It is connected between the CUT and ground. In a defect-free state, the virtual ground Vgnd point is at "0" where T1 is turned "on" and T2 is "off", In the presence of a fault, the defective current is drawn by the CUT, and the increased Vgnd voltage turns T1 "off" and T2 "on". This voltage level is compared to the Vref value by the flip-flop. The result is the PASS/FAIL signal at the monitor output. In case of a high current resulting from the shorts between the "power supply" point and "ground" point, the circuit breaker turns off the T4 and disconnects the CUT from the power supply. Transistor T3 ensures the correct operation of the circuit breaker by restoring the voltage at Vgnd.

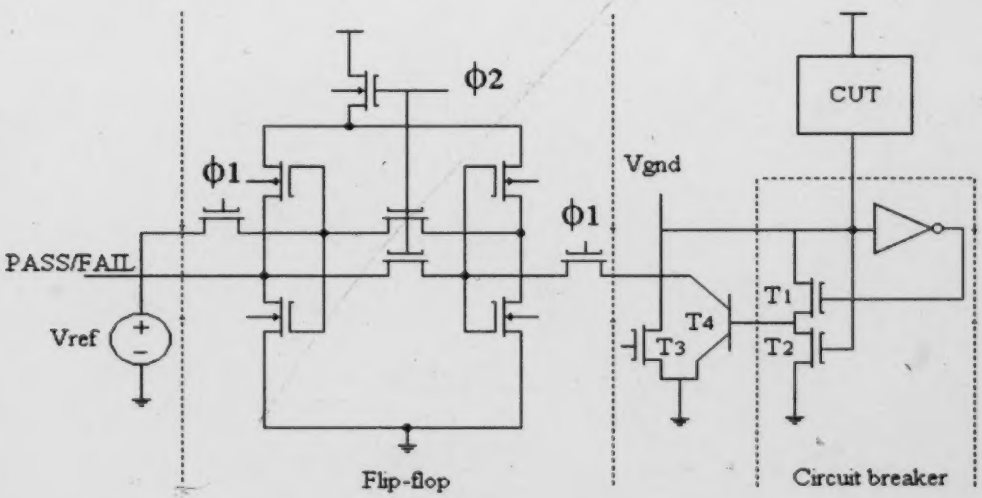

Figure 2.16: Monitor proposed by Maly et.al.

A great deficiency of this design is the position of the monitor between the CUT and ground point. This position introduces a virtual ground point affecting the circuit's

performance. Another drawback is the requirement of a two-phase clock. Finally, the lateral NPN BJT used in the design makes this circuit difficult to implement.

Monitor Design proposed by Miura

This is an example of a direct monitor [24]. The two voltage sources supply CUT through two diodes. The monitor design is shown in the Figure 2.17. The current is mirrored to the delay circuit preventing false error signal due to a dynamic current during switching. The main drawback of the circuit is the requirement of two power supplies, which make the monitor impractical for the most of the applications.

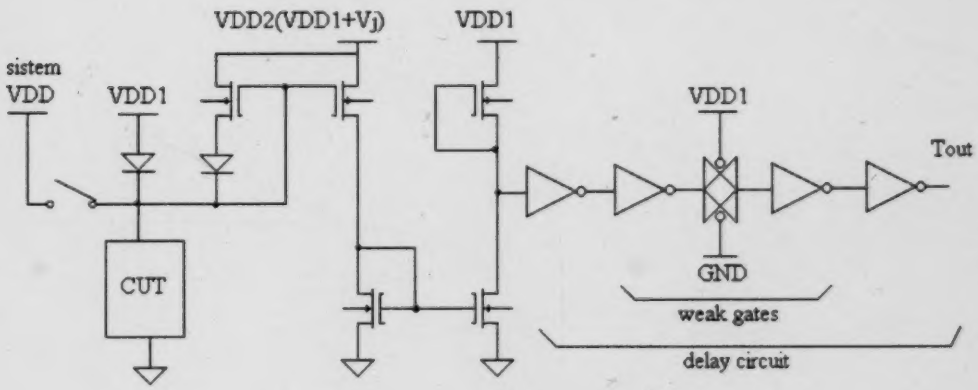

Figure 2.17: Monitor Design by Miura

Monitor Design proposed by Tang

The current sensor is made of a two-stage operational amplifier (OPAMP), a threshold voltage detector and a resistor [25]. The monitor is shown in Figure 2.18. The CUT current passes the resistor Rs and produces the voltage drop on Rs. This voltage drop is sensed by the Threshold detector. A signal "Fault" is produced each time the current goes over the predefined threshold value.

The main disadvantage is the additional power supply Vdd' required for the operation of an operational amplifier. The Vdd' should be higher than the CUT power supply. As well, the characteristics of the OPAMP are difficult to implement accurately.

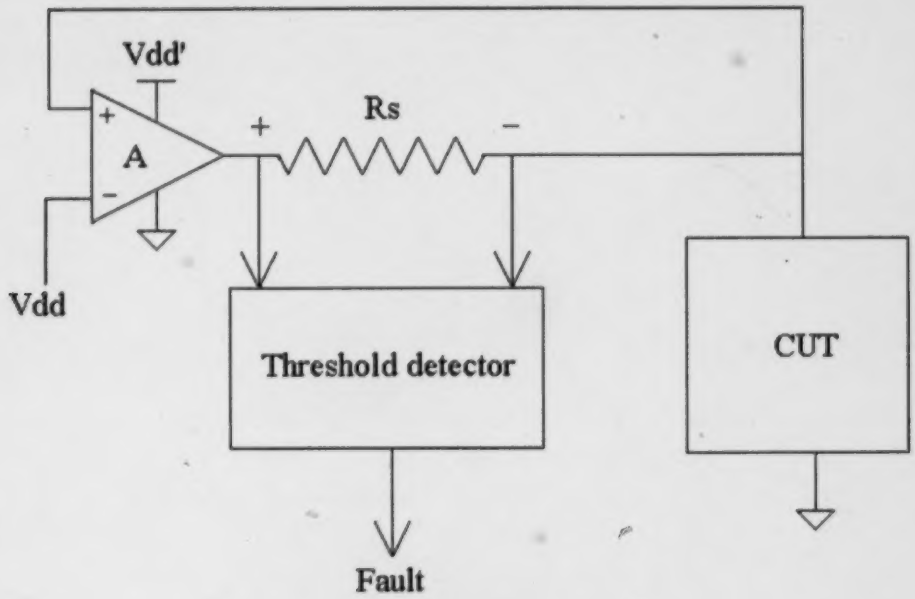

Figure 2.18: Monitor proposed by Tang

Monitor Design proposed by Kim et.al .

The essential element of this monitor is the current mirror [14]. See Figure 2.19. The current of the circuit-under-test is mirrored and compared to the reference current. If the CUT current is larger, then the reference current PASS / FAIL signal is set to "1", indicating the presence of a fault. The function of Q_0 is to connect or disconnect the monitor. Transistor Q0 is controlled by the TCLK signal and turned off as soon as CUT reaches the quiescent state. As a result, the dynamic current produced by the CUT has no effect on the monitor since it is sinked through the Q0 during the switching period.

The monitor is inserted in series between the circuit-under-test and the ground and suffers from the same deficiency as the Maly design. In order to be able to sink large transient currents, the transistors have to be large, introducing a large capacitance and an extra

delay. This factor may also cause a ground-bounce problem and seriously affect the functionality of the CUT. Signal EXT is applied to solve the problems of parasitic capacitance and ground bouncing providing the ground point in normal operation and floating during the test mode.

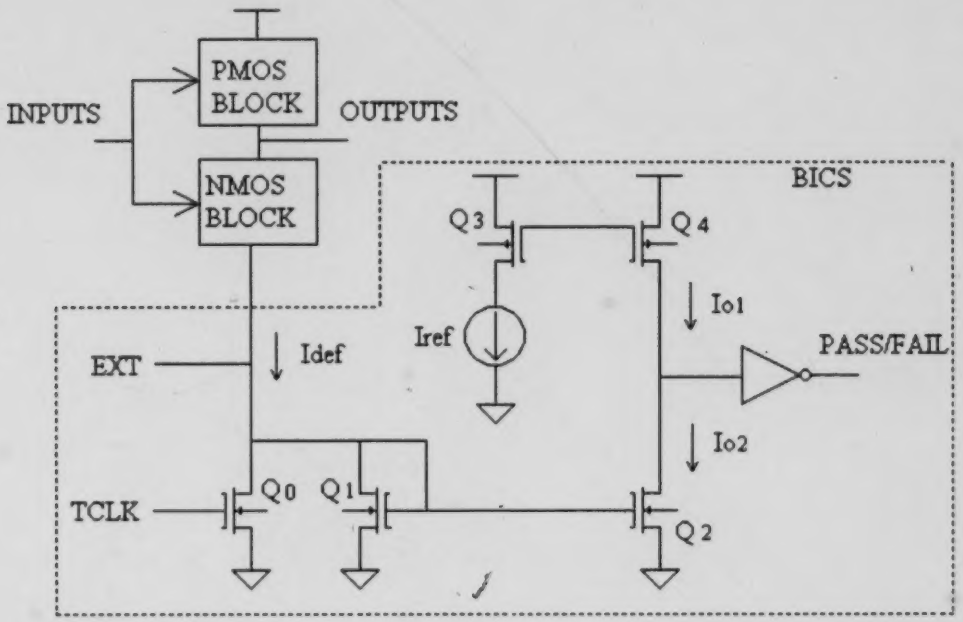

Figure 2.19: Monitor proposed by Kim and Hong

Conveyor Based Monitor proposed by Stopjaková et.al.

An interesting example of Iddq testing design is shown in the Figure 2.20 [26]. A CCI+ current conveyor is used as a monitor. The results obtained are shown in Table 1. Investigate range of currents was from 50 nA to 10 μA with the testing frequency of 100 kHz and C_{LOAD} = 50 pF. CCI+ current conveyor has two main functions in the design. One is to convey the I_{DD} current to the output terminal and the other is to keep the voltage level at the both input terminals. During the switching the circuit produces high transition currents and the Bypass circuit is added to protect the monitor. At the output I_{DD} current

is compared to the reference value I_{ref} at the current comparator and the signal Flag is produced as a result of the comparison. Since this is done continuously, this signal is then sampled at the end of the measurement period.

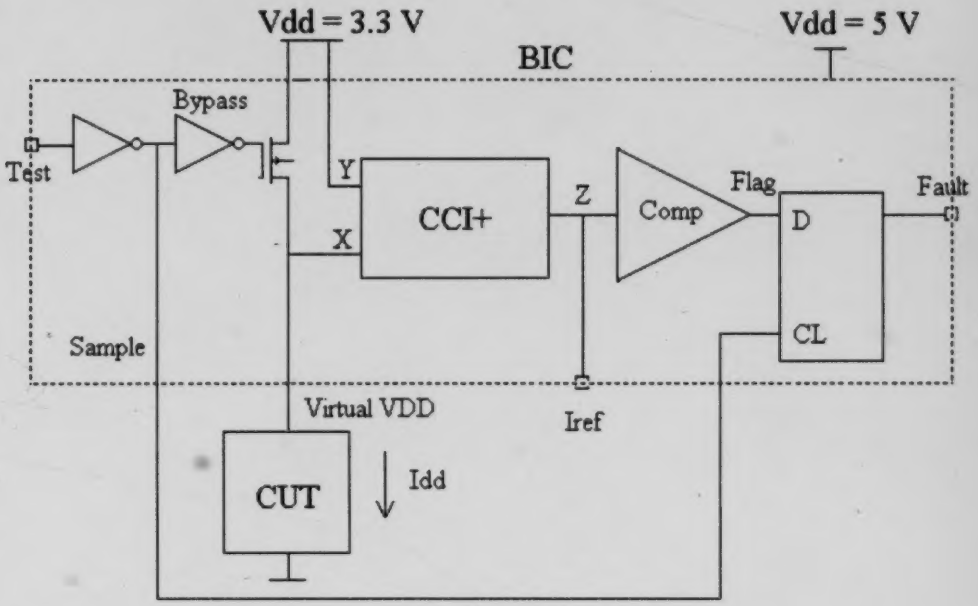

Figure 2.20: Monitor proposed by Stopjaková et.al.

As we can see, accuracy depends on the value of the current and the best results are obtained for the currents in the range 1 μA to 100 μA. Unfortunately the paper from this research did not provide any data on fault coverage.

Table 2. 6: Iddq test accuracy results

Iddq current	Measured Iddq	Accuracy
50 nA	43 nA	14 %
100 nA	92 μA	8 %
1 μA	0.98 μA	2 %
10 μA	9.99 μA	0.1 %
100 μA	100.3 μA	0.3 %
600 μA	550 μA	8.3 %

Monitor Design proposed by Antonioly et.al.

The main idea for this monitor was to amplify voltage drop initially caused by the current flowing through the current-to-voltage translator inserted between the CUT and the power supply [27]. The schematics of the monitor can be seen in Figure 2.21. Diode D limits the voltage drop produced from large transient currents. Tp1 and Tn1 use as a voltage shifter the sensed voltage to a Vshift_cut. This voltage is further amplified by the inverter. The use of a depletion type P-MOS transistor in a level shifter allows for good sensitivity of voltage levels nearly equal to Vdd, so that only one power supply is sufficient. Large Rsens produces a large supply voltage deviation and, for large transient currents, affects Iddq settling time. The biggest drawback is that extra process steps are required to manufacture depletion type transistor Tp1.

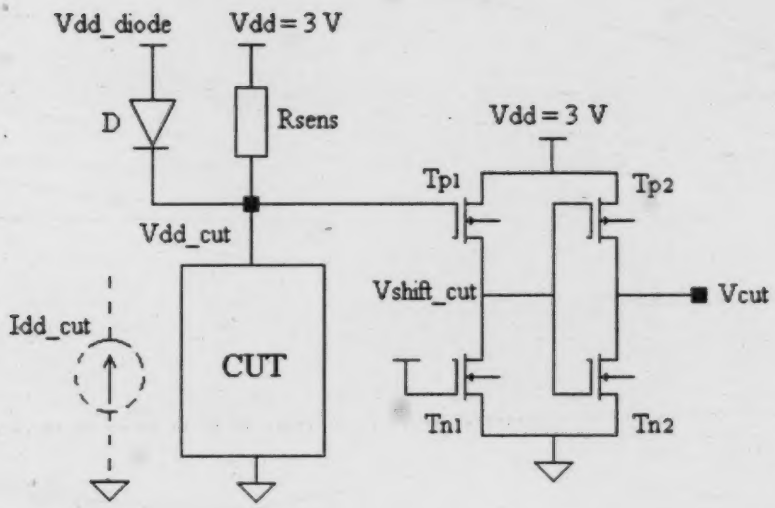

Figure 2.21: Monitor proposed by Antonioli and Kinoshita

Monitor Design proposed by Maidon et.al.

This monitor is based on the idea of the parasitc resistance of the metallic interconnection layer [19]. See Figure 2.22. In fact, aluminum used to connect the core to a die always induces a small parasitic resistor. It is assumed that this value is around 1Ω. Idd current flowing into the CUT produces a voltage drop on this parasitic resistance and results in an unbalanced current mirror. At the output of the current mirror, Imeas is linearly proportional to the Idd current drawn by the CUT. Since Imeas is several orders lower than the Idd, a current amplifier is used to amplify the output current signal.

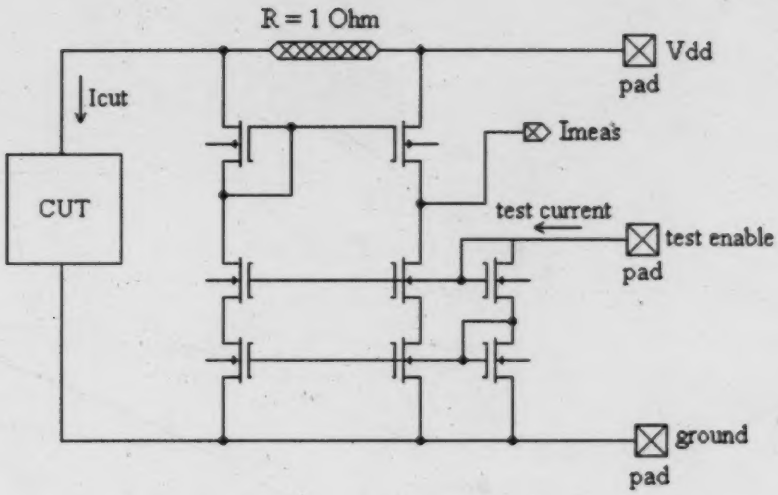

Figure 2.22: Monitor proposed by Maidon et.al.

Current Mirror Based Monitor Proposed by Stopjaková et.al.

This proposed monitor implements the previous idea of an unbalanced current mirror (Figure 2.23) [28]. Design of the current mirror is classic, replacing the cascode design used in the previous monitor. High transient peaks of the mirrored supply current Imir pass through the diode D and charge capacitor Ccharge. The voltage value of the charged capacitor is compared to the reference value. This design suffers from two drawbacks: the non-linearity of the diode D, and the sensitivity of the amplifier. Authors report high accuracy of the monitor in the range of several μA's to 100 mA's.

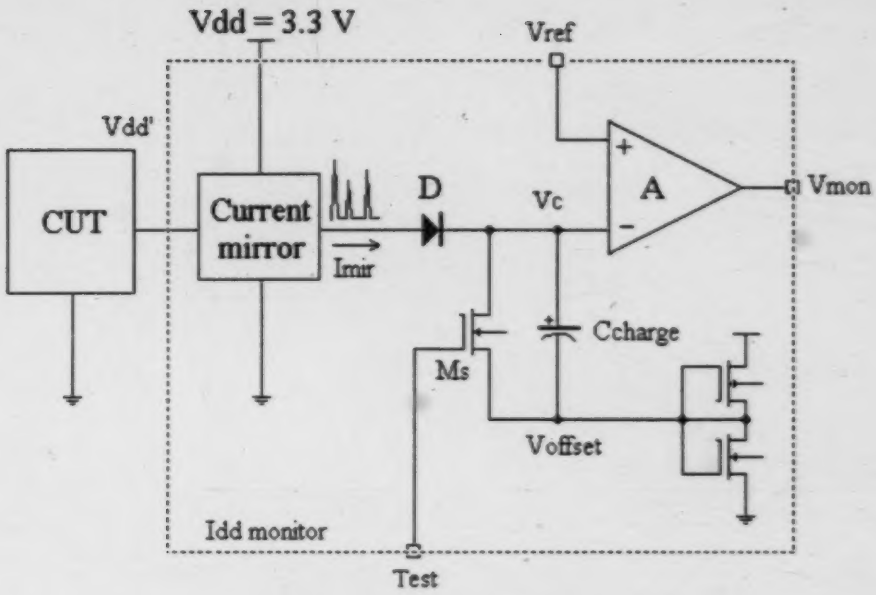

Figure 2.23: Monitor proposed by Stopjaková et.al.

Most of the presented monitors are Iddq monitors. Stopjaková/Manhaeve monitor, designed for Iddq testing, suffers from low sensitivity. Improvement of this design, Monitor 1, is described in the next chapter.

Chapter 3

Current Monitor 1 Design[1]

This chapter describes an improved version of the Stopjaková/Manhaeve monitor design. This design is named "Monitor 1" since it is the first of the two monitor designs presented in this thesis [29]. The design is implemented in different technologies (0.35 μm and 0.5 μm) and in a Low-Voltage Environment (1.5 V). The first section presents the scheme of the Monitor 1. The design of the current mirror, the monitor's main part, is presented in Section 3.2. The A/D converter is described in Section 3.3. Section 3.4 explains the design of the comparator. The CUT used in testing the current monitor is described in Section 3.5. Simulation results and test results are given in Sections 3.6 and 3.7, respectively. Possible options for signal processing are discussed in 3.8. Circuit implementation in both 0.5 μm and 0.35 μm technologies is given in Section 3.9. Finally, Section 3.10 analyzes the advantages and drawbacks of the Monitor 1 design.

[1] Part of this chapter has been published in the "1.5 Volts Iddq/Iddt BIC Monitor", Proceedings of the IEEE Canadian Conference on Electrical and Computer Engineering, pp. 472-476, 1999.

3.1 Monitor 1 Design Scheme

The main elements of the current monitor are Resistor R, current mirror, diode D, capacitor C, switching circuitry and fast A/D converter. The monitor design is shown in Figure 3.1. The resistor R is inserted in series with a CUT. The power supply current passing the resistor R produces a voltage drop on R. This voltage drop disbalances the current mirror, resulting in an output current Iout. This current passes the Diode and charges the capacitor C to the voltage Vc. This way, the current signal is converted to the voltage signal. After the sampling, a short pulse of the Test signal is applied to discharge the capacitor and to prepare it for the next sampling. The diode has an important function of cutting the reversing current signal off when the current drops at the end of the pulse. Without the diode, the same signal would charge and shortly after discharge the capacitor without producing any signal Vc. The sampled voltage Vc is further digitized on a fast A/D converter. The end result of an Idd current signal conversion is a digital value easy to process and to evaluate.

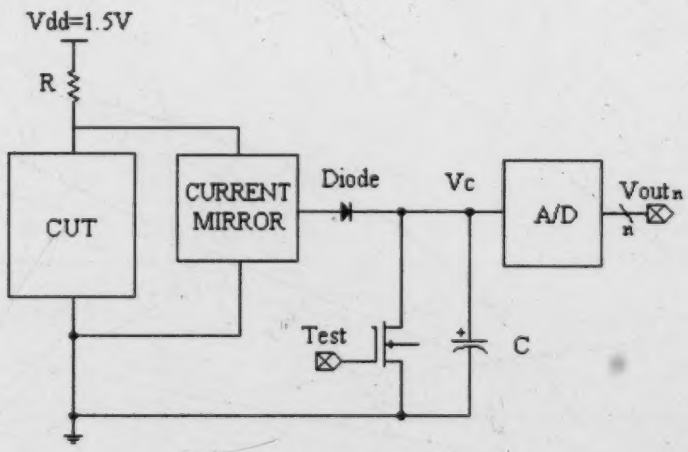

Figure 3.1: Proposed Monitor 1 Scheme

The monitor's most important part is the current mirror. Its design is shown in Figure 3.2. Any current mirror operates on the following principle: as a result of identical

voltages at the gate-source of a transistor pair (MP1/MP2), $Vsg_1 = Vsg_2$, the current through transistor MP1 is mirrored to the transistor MP2 in relation expressed in the formula:

$$\frac{Ip_1}{Ip_2} = \frac{W_1}{W_2} \tag{3.1}$$

where W1 and W2, respectively are widths of the transistor pair. Equation (3.2) describes the saturation current flowing through the PMOS transistor:

$$Idp = \frac{1}{2}\mu_p Cox \frac{W}{L}(Vsg - Vtp)^2 \tag{3.2}$$

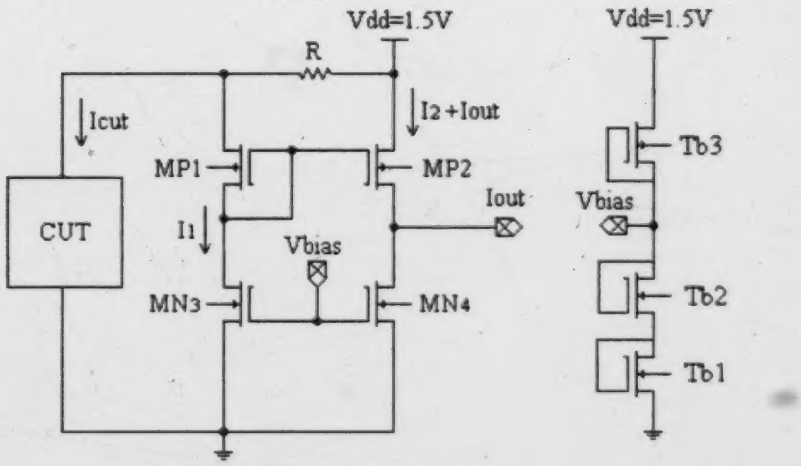

Figure 3.2: Current mirror.

In order to achieve normal operation of the current mirror, all transistors have to be in saturation. The requirement for a PMOS-transistor to operate in a saturation mode is

$$Vsd \geq Vsg - |Vtp| \tag{3.3}$$

In the proposed design, Resistor R as a sensing element is inserted between the current mirror's branches. Due to the current flow through these branches, a voltage drop is induced on R, resulting in different gate-source voltages of a transistor pair and unbalancing the current mirror:

$$Vsg_2 > Vsg_1 \quad results\ in \quad I_2 > I_1 \tag{3.4}$$

where

$$Vsg_2 = R\,(\,Icut + I_1\,) + Vsg_1 \tag{3.5}$$

MP2 is more open and passes more current than MP1. This excess current is actually the output current - Iout. Extracting the Iout from formula (3.1) (3.2) (3.4) and (3.5), we obtain equation (3.6):

$$Iout = R(2\mu_p Cox\frac{W}{L}I_1^3)^{1/2}(1+\frac{Icut}{I_1}) \tag{3.6}$$

Since Iout is several orders of magnitude lower than Icut, this current is difficult to use without amplification. Nevertheless, parametric simulation with a range of C values proved that if a very small value of C is used (less that 0.5 pF) a Vc signal up to 1 V can be obtained. The advantage of using a small capacitor is the shorter charging and discharging time of the capacitor. This advantage significantly improves the monitor speed and a testing speed of 80 MHz can be obtained.

Another important element of the monitor is the resistor R. The designs proposed earlier [21] based on the same principle, use the small parasitic resistance of the interconnection layer between the core and I/O pads (assumed to be around 1Ω). A serious drawback is that a low value of R gives poor sensitivity of the device for the Idd currents in the order of mA.

Two criteria were used in the determination of R value:

- Supply-voltage degradation, produced during transient current peaks ($I_{peakmax}$), should be less then 5%, i.e., $I_{peakmax} R < 0.05\ Vdd$.
- In order for the current mirror to operate correctly, transistors MP1 and MP2 should be always in saturation, i.e., $Vsg < Vsd + Vtp$.

3.2 Current Mirror Design

The current mirror is the main part of the Monitor 1 design and it is based on the PMOS transistor pair structure. Another option in the monitor's design was to use NMOS transistor pair current mirror, but simulation results indicated that NMOS based current mirror exhibits more negative impact, such as ground bouncing, on CUT performance.

The design started with a selection of the length of the devices to be used in the mirror. A length of 1 μm was chosen in order to avoid short channel effects. Second, the bias voltage Vb = 1 V and width of NMOS transistor pair, $W_{3,4}$ = 10 μm, were selected. The selection of the biasing voltage Vb defined currents through the current mirror I_{mir}:

$$\mathrm{Im}ir = \frac{1}{2}\mu_p Cox\frac{W}{L}(Vgs - Vtn)^2 = 139.86\mu A, \qquad (3.7)$$

where V_{tn} = 0.6 V, θ_n = 0.63, μ_nCox = 200. In order to mirror large current values, the width of PMOS pair W = 200 μm was selected. The large size of the PMOS transistor pair is one of this design's drawbacks. Biasing circuitry was built with two NMOS transistors (Tb1 and Tb2 in Table 3.1) and one PMOS transistor (Tb3 in Table 3.1) connected in series. Table 3.1 with the sizes of device in the current mirror is given below.

Table 3.1: Current mirror device sizes

DEVICE	WIDTH	LENGTH
PMOS TP1	200 μm	1 μm
PMOS TP2	200 μm	1 μm
NMOS TN3	10 μm	1 μm
NMOS TN4	10 μm	1 μm
NMOS Tb1	1 μm	2.5 μm
NMOS Tb2	1 μm	2.5 μm
PMOS Tb3	20 μm	1 μm

Special attention has been paid to the layout of the current mirror. Large PMOS transistors are split into parallel devices in order to reduce resistive parasitics resulting from long interconnecting lines and capacitive parasitics resulting from a reversed-biased diffusion substrate diode. The current mirror layout is given in Figure 3.3.

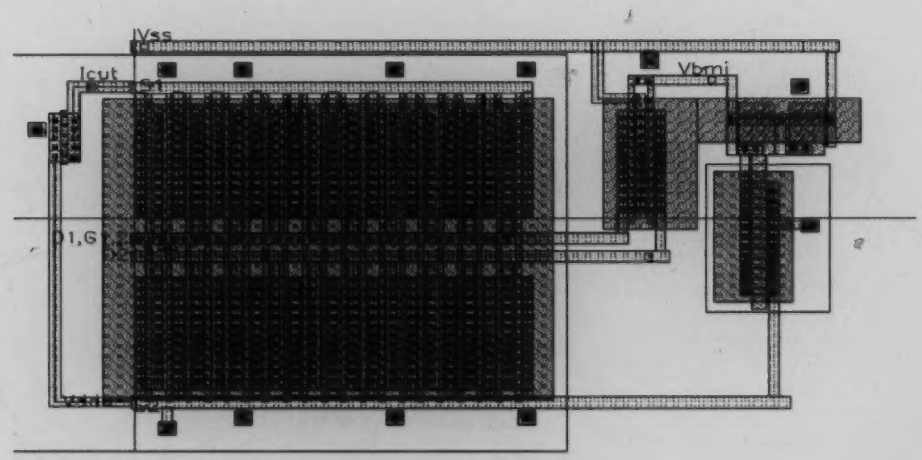

Figure 3.3: Current mirror layout

3.3 A/D Converter

Vc value is digitized on a fast flash A/D converter. The converter consists of a series of 5 resistors and 4 comparators, as shown in Figure 3.4. Comparators are the limiting factor in obtaining higher speed, so special attention has been paid to the design layout in order to obtain a lower speed degradation.

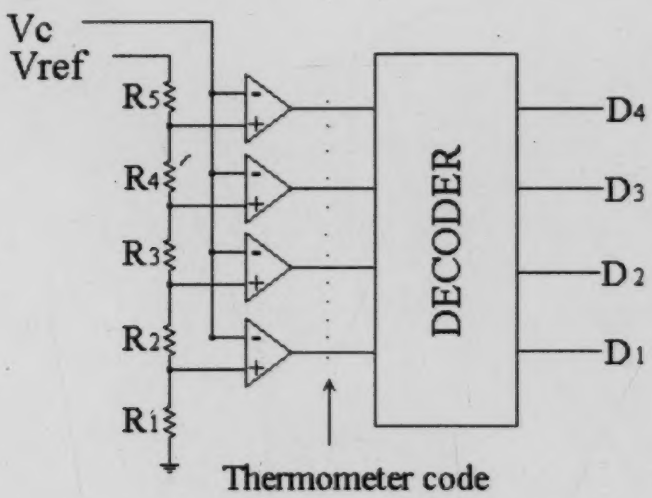

Figure 3.4: Flash A/D converter

This A/D converter differs from conventional converters. The converter's voltage levels are not distributed equally over the whole range of the Vc values. An example of the distribution of the reference voltage values for an 4-bit A/D converter is shown in Figure 3.5. One value is asserted to $Iddq_{max}$ (V0 in Figure 3.5) and detects the presence of the excess leakage current -- Iddq. Other values (V1 - V3 in Figure 3.5) are distributed between Iddmin=V1 and Iddtmax=V3 values, so that the presence of the pulse can be detected more efficiently.

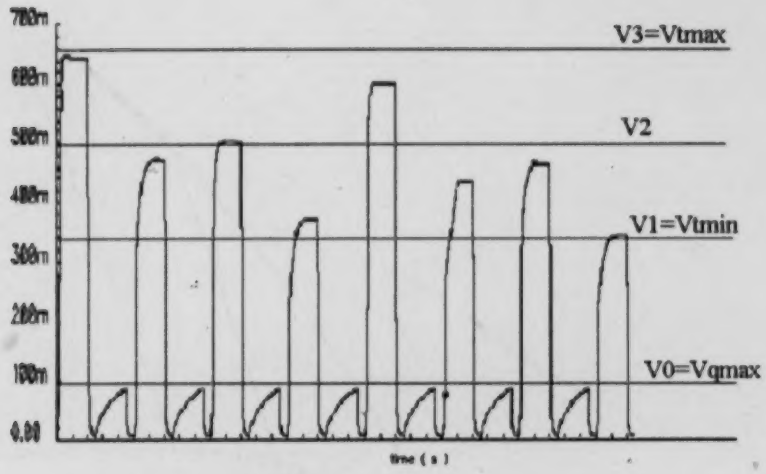

Figure 3.5: Example of A/D converter voltage references

3.4 Comparator Design

The main part of the A/D converter is the comparator. Figure 3.6 shows a comparator's design. Design of the comparator started with the selection of the bias voltage Vbias=0.5 V. As in the design of the current mirror, the lengths of the devices are 1 μm. the width of the biasing transistor is chosen as W=17 μm. The current Ibias is defined by equation (3.8):

$$Ibias = \frac{1}{2}\mu_p Cox\frac{W}{L}(Vsg - Vtp)^2 = 67.03\mu A, \qquad (3.8)$$

(where $V_{tp} = 0.7$ V, $\theta_p = 0.43$, $\mu_p Cox = 70$). Bias circuitry is made of Tbp and Tbn transistors connected in series.

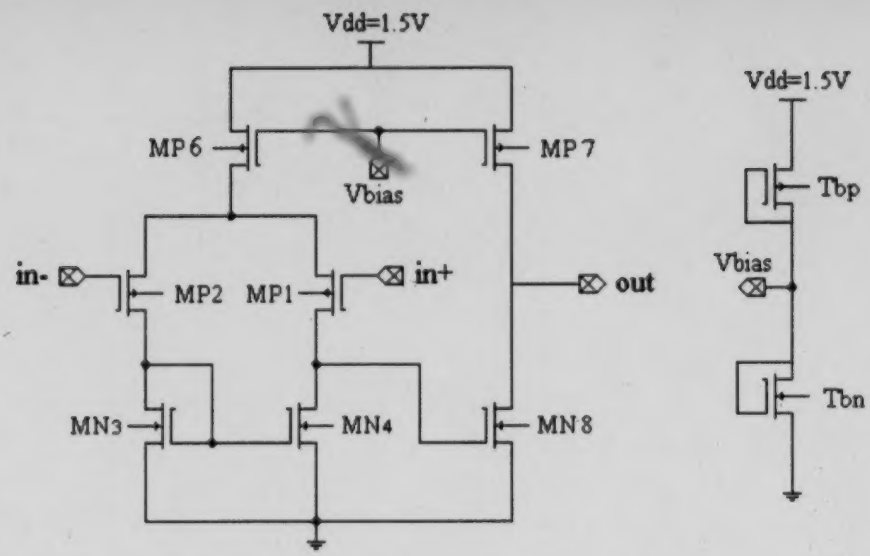

Figure 3.6: Comparator schematics

Table 3.2: Comparator device sizes

DEVICE	WIDTH	LENGTH
PMOS MP1	40 µm	1 µm
PMOS MP2	40 µm	1 µm
NMOS MN3	10 µm	1 µm
NMOS MN4	10 µm	1 µm
PMOS MP6	17 µm	1 µm
PMOS MP7	17 µm	1 µm
NMOS MN8	30 µm	1 µm
PMOS Tbp	17 µm	10 µm
NMOS Tbn	10 µm	17 µm

The layout of the comparator is presented in the Figure 3.7.

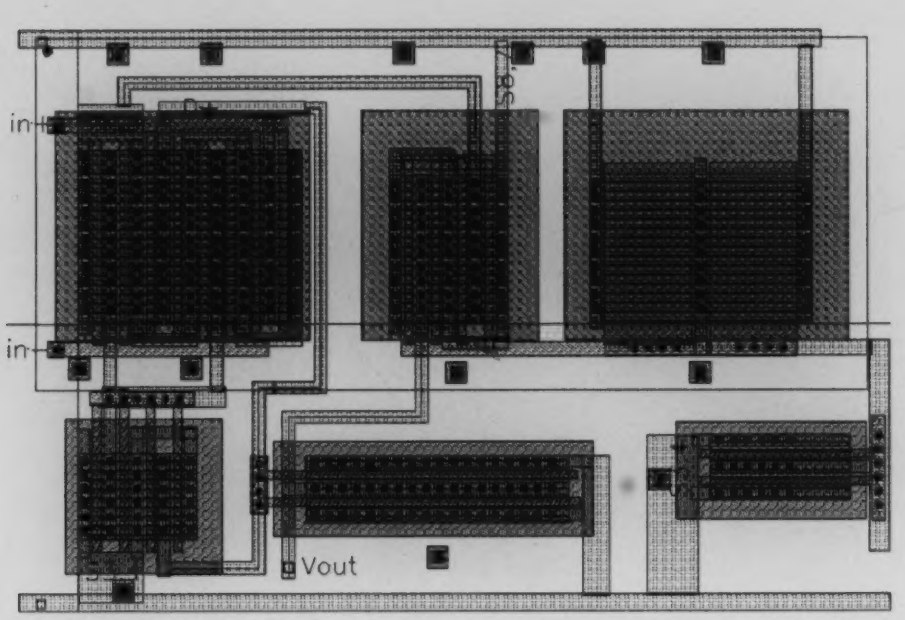

Figure 3.7: Comparator layout

3.5 CUT – Circuit-Under-Test

Sets of chains of inverters have been used as the CUT. Figure 3.8 shows the CUT design. A series of 30 inverters is connected in 9 parallel lines. The Vin signal is supplied to the front end. Two types of faults are simulated in order to check the monitor performance - open fault and a short fault. An open fault is simulated using the transistor as a switch (F_{open}) to disconnect a part of the circuit. The switch transistor (F_{short}) connects one of the output lines to the ground and simulates a short fault.

The resistor of value 300 Ω was connected in series with a shorting transistor because, statistically, most of the short faults introduce a fault path of resistance less than 500 Ω.

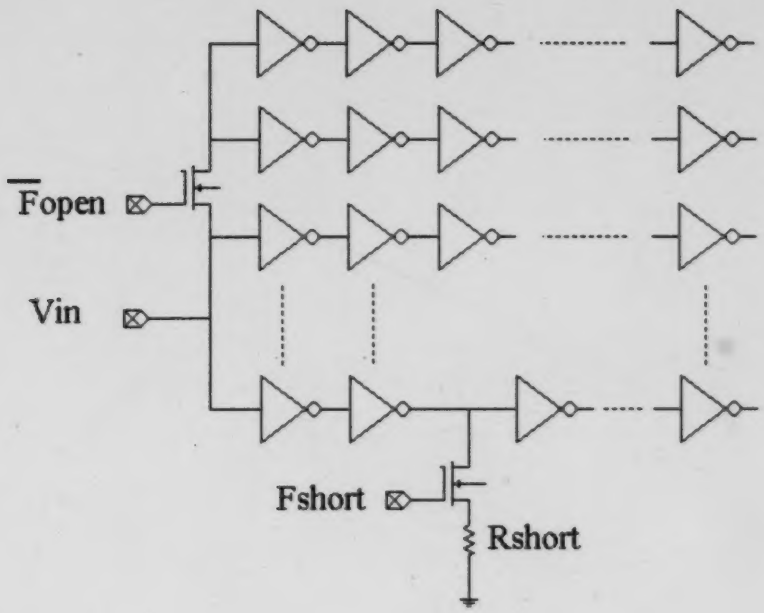

Figure 3.8: Circuit under test (CUT)

3.6 Simulation Results

0.35 μm design: Other values used in the simulation were: Vc= 0.3 pF and R=1Ω. First, the circuit was tested with an input signal of the frequency f=1 MHz. The circuit's transient response is depicted in Figure 3.9. As shown in the graph, an open fault was activated first, affecting 30% of the circuit. The monitor successfully detected the fault. The absence of digital pulses indicated a lower current response during the period of active open fault. When the shorting transistor is turned on, the current signal is increased and the difference detected.

After this, the monitor is tested for its maximum speed. Due to the RLC effects, a 100 MHz speed is defined as the top limit, where the monitor is still able to produce some response pattern. The transient response is shown in Figure 3.9, which reveals how V3 is

distorted and V1 and V2 outputs are stuck at high because of the difficulty of following the high-speed signal.

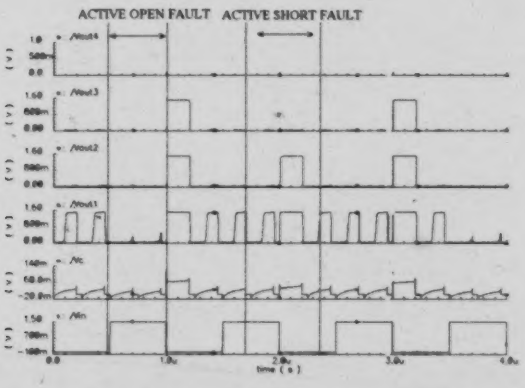

Figure 3.9: Monitor transient response (1 MHz)

(bottom-top: Vin, Vc, V1-V4)

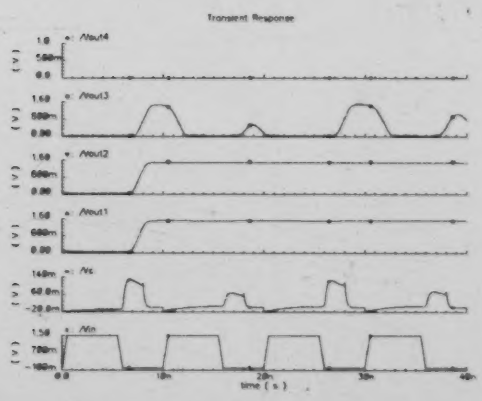

Figure 3.10: Monitor transient response (100 MHz)

(bottom-top: Vin, Vc, V1-V4)

0.5 μm design: This design was implemented with only one bit A/D converter and basically only one Fault / No-fault signal. The monitor response for the clock speed of 1 MHz is shown in Figure 3.11, which reveals the difference between the no-fault monitor

response during the first clock signal and the fault response during the second clock signal (active open fault).

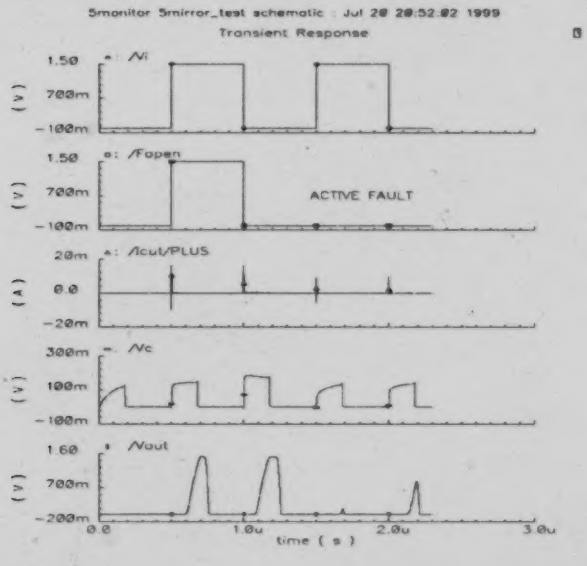

Figure 3.11: 0.5 μm Monitor transient response (1 MHz)

(bottom-top: Vout, Vc, Idd, Ffault, Vin)

The highest speed at which the monitor was able to operate was 25 MHz. The critical factor was the comparator's speed in the AD converter design. A delay of the comparator of about 150 nsec limited the monitor's overall speed.

3.8 Signal Processing

The monitor's final output is in the digital form and is easy to evaluate and process either internally--on chip or externally--off chip.

On-chip processing has the advantage of requiring fewer pins for the signal output. One pin with an Fault signal is sufficient. Several options exist for a monitor output analysis. The option if using a memory block, which would contain the correct response for the selected set of input vectors, would increase the size of the testing circuitry. Another option is to use a signature compactor and decrease the number of required output pins. The third option of using combinational circuitry such as a decoder and to comparing the monitor's response with the corresponding input vector would be feasible only for a small CUT with a small number of test vectors.

In any case, dealing with the digital output provides more options in detecting the fault. The proposed technique clearly provides a much greater possibility of fault detection with high accuracy then does the present current testing techniques, which use only one reference value of the power supply current.

3.9 Circuit Implementation of Monitor 1

The monitor was implemented in 0.35 μm technology and 0.5 μm technology. The actual layouts in both technologies are shown in Figure 3.12 and Figure 3.13. The circuit was fabricated with cooperation from Canadian Microelectronics Corporation (CMC).

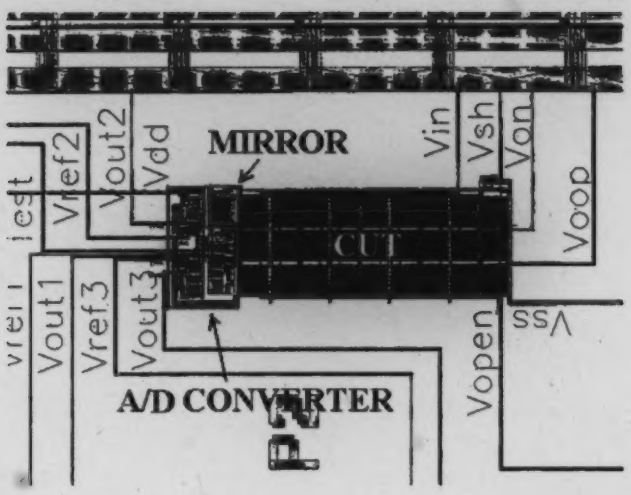

Figure 3.12: Layout of the Monitor with CUT - 0.35 μm

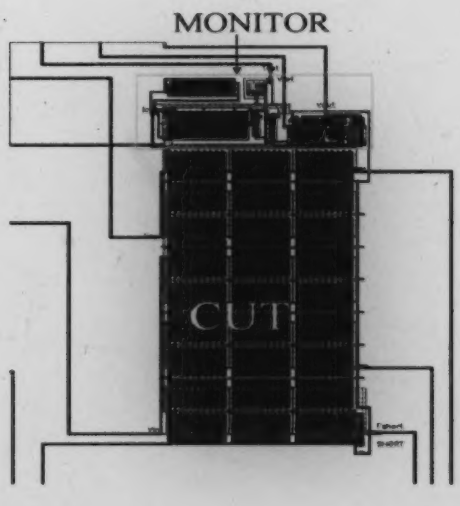

Figure 3.13: Layout of the Monitor with CUT - 0.5 μm

The area of the CUT (series of inverters) is 45,900 μm^2 for the 0.35 μm design and 59,400 μm^2 for the 0.5 μm design. The area of 0.35 μm current monitor design,

including the 3-bit A/D converter, is 8,340 μm^2. The resulting area overhead required for the monitor for this particular example of CUT is 15 %. The monitor area of the 0.5 μm design is 10200 μm^2, which results in 18 % overhead.

3.10 Advantages and Disadvantages

This monitor design has several advantages compared to the similar designs used for current monitoring. This monitor design is intended for operation in a Low-Voltage environment (1.5 V) and is able to detect open and short faults that escape traditional voltage-type testing. The monitor can be used for both types of current monitoring: quiescent and transient. It can also be used on circuits with high testing speed. The impact on the circuit under test is minimal. The actual design is relatively simple, with small number of devices.

The greatest drawback is the silicon area required for the design. The largest contributor is the A/D converter. The second disadvantage is the inability to detect high speed changing pulses shorter then 300 psec. The use of a small Vc value can make this circuit prone to the effect of parasitic capacitance.

3.11 Test Results

A test bench was set up for testing the Monitor 1 circuit. The list of the instruments and equipment used during the testing is given below. The test environment is shown on Figure 3.14.

Test equipment:

- breadboard
- CQFP 44-pin chip socket
- Two Tektronix TDS220 -- Two channel Digital Real-time Oscilloscope
- Hewlett Packard 8111A Pulse/Function Generator 20 MHz
- Hewlett Packard 33120a 15 MHz Function / Arbitrary Waveform Generator

- BK PRECISION 4 ½ digit True RMS Multimeter Model 2833
- BK PRECISION Triple Output DC Power Supply 1651
- Hewlett Packard 6227B Dual DC Power Supply
- Hewlett Packard E2373A Multimeter
- Banana leads

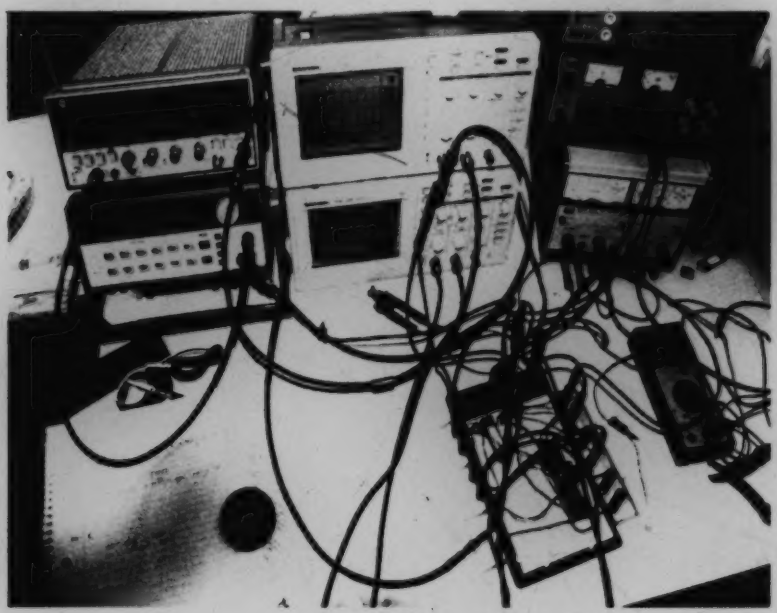

Figure 3.14: Test environment

A HP33120A signal generator was used for the circuit's square wave input signal. A HP8111A provided narrow Test signal used for the switching circuit. Both input signals had to be synchronized, so the output of the HP33120A was fed into the external input of the HP8111A signal generator. As well, the HP 8111A was set to the Trigger mode. The width of the Test signal was varied by the DUTY / WIDTH control.

The delay of the signal generators was measured. At 100 kHz input signal speed, the delay of the rising edge was t_{dr} = 33 nsec, and the falling edge delay was d_{tf} = 40 nsec. At 1 MHZ the signal had a delay of t_{dr} = 37 nsec and d_{tf} = 45 nsec.

The signal speed was varied in order to obtain the monitor's maximum operating speed. It was found that monitor was able to operate with the maximum speed of 1 MHz.

It was also observed that poor testing environment with long interconnecting wires and banana connectors introduced large resistive, capacitive and inductive parasitics. This was main limiting factor in obtaining better test results. As well, various power-supply values were applied to the circuit. Figure 3.15 and Figure 3.16 show circuit responses at 100 kHz and 1 MHz with 1.5 V power supply, respectively. A varied the DC Power supply produced a circuit operation range between 1.46 V and 2.1 V. Figure 3.17 and Figure 3.18 show circuit response at 100 kHz and 1 MHz with 2 V power supply, respectively.

Monitor performance was tested by activating the open-fault. When the open-fault was active, 30 % of the CUT was not operating and less current was drawn by the CUT. The monitor was able to detect the fault creating the High/Low output signal.

A sample set of 10 chips was tested sequentially in order to monitor parameter variations. Since no parameter variation was observed, it was concluded that the external parasitics' high influence did not allow for observation of these variations.

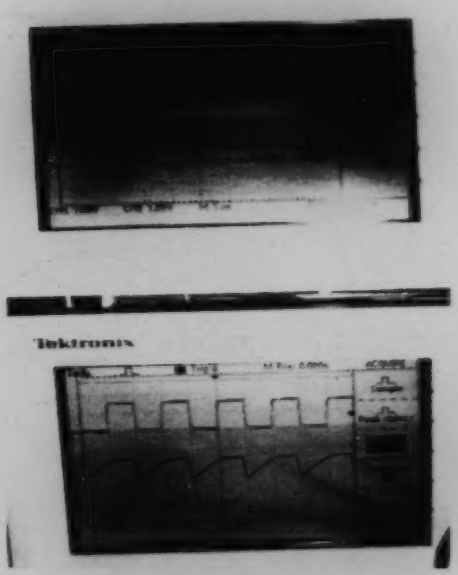

Figure 3.15: f=100 kHz / Vdd=1.5 V

(top/bott.: Vin, Test, Vout, V1)

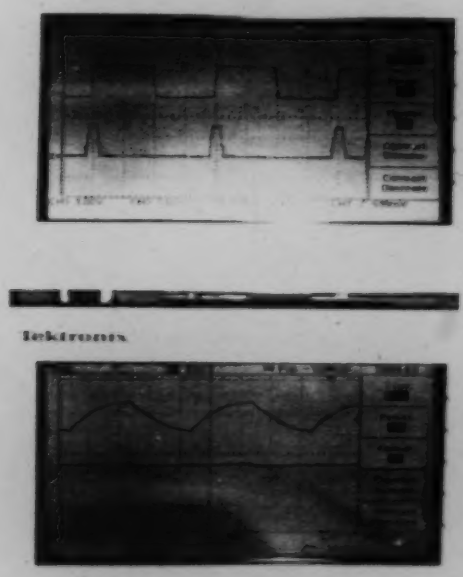

Figure 3.16: f=1 MHz / Vdd=1.5 V

(top/bott.: Vin, Test, Vout, V1)

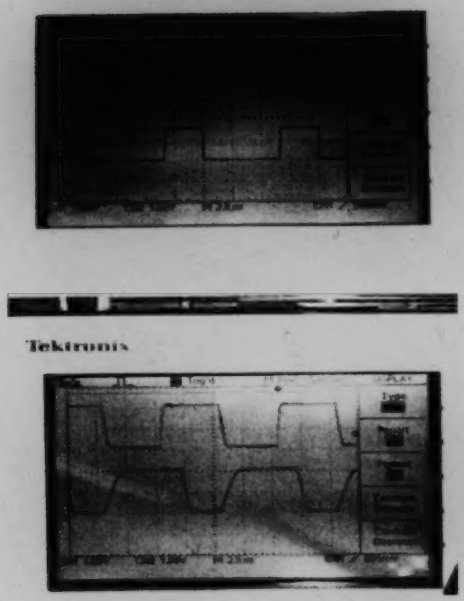

Figure 3.17: 100 kHz / 2 V

(top/bott.: Vin, Test, Vout, V1)

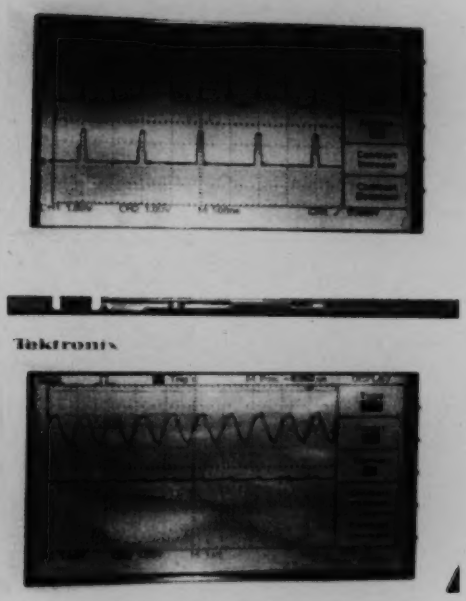

Figure 3.18: 1 MHz / 2 V

(top/bott.: Vin, Test, Vout, V1)

Chapter 4

Current Monitor 2 Design[2]

This chapter proposes a new monitor for On-line current testing, incorporating both Iddq and Iddt monitoring capabilities. Like Monitor 1, Monitor 2 is also based on the mechanism of an unbalanced current mirror [30,31]. Monitor 2 performance is improved by adding the second current-sensing element, which increases sensitivity resolution. The design can also be applied to test Mixed-Signal circuits. Section 4.1 gives design details. Section 4.2 explains the design of the current mirror. Section 4.3 provides simulation results. This Section has two parts. Section 4.3.1 analyzes results of monitor application to the digital circuit, and Section 4.3.2 analyzes results of monitor application to the mixed-signal circuit. The implementation of the circuit in 0.35 μm technology is shown in the Section 4.4. Section 4.5 briefly refers to the possibilities of the signal processing, and Section 4.6 presents test results.

4.1 Monitor 2 Design Scheme

A novel Idd built-in current (BIC) monitor for concurrent Iddq and Iddt testing is proposed in order to implement advantages of both (Iddq and Iddt) testing techniques and augment the testing capabilities of the current monitor.

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[2] The part of the material in this chapter is published in: "Low-Voltage/Low-Power Iddq/Iddt Current Monitor for On-Line Testing", Proceedings of 5th International Mixed-Signal Testing Workshop, pp.67-72, 1999, and "0.35 μm 1.5 Volts Iddq/Iddt Current Monitor", Proceeding of the IEEE European Test Workshop, CD ROM 1999,

The proposed design consists of two sensing elements, resistors Rp and Rn, a current mirror, a diode, a capacitor and a fast A/D converter (Figure 4.1). This design is similar to the design of Monitor 1, with the addition of a second sensing element, resistor Rn. This resistor has two important functions: it increases the Iout, output current of the current mirror, which is directly proportional to the Icut, current of the CUT and it controls offset current of the current mirror. The operation of the Monitor 2 is similar to that of Monitor 1.

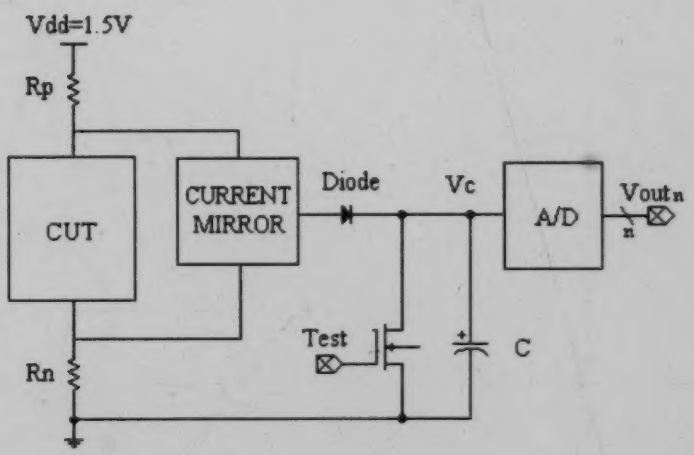

Figure 4.1: Proposed Monitor 2 scheme

A power supply current, passing through the CUT produces a voltage drop on Rp and Rn. This voltage drop unbalances the current mirror from both sides, the PMOS transistor pair side and the NMOS transistor pair side, resulting in the current Iout at the current mirror output. The Iout passes through the Diode and charges the capacitor C. As with Monitor 1, we obtain voltage signal Vc, which corresponds to the current drawn by the CUT. The Test input is used for sampling the Vc voltage. Concurrent monitoring of the Iddq and Iddt part of the power-supply current can be obtained by selecting the appropriate Test signal. Test signal "low" enables charging of the capacitor C during the switching phase of the CUT, after an input signal has been applied to the CUT, and

during the quiescent phase of the CUT, when power supply current has settled down. Narrow "high" Test pulse is provided to discharge the capacitor and prepare the monitor for the next Iout current signal. The sampled Vc voltage is then digitized on the fast flash A/D converter, and at the output of the converter we receive the digital signal, which is easy to evaluate and process.

4.2 Current Mirror Design

Figure 4.2 illustrates the current mirror's operating principle. Two sensing elements, resistors Rn and Rp, are inserted into the Idd path. The Idd current, drawn by the circuit under test produces a voltage drop on both resistors and unbalances the current mirror on both sides. The higher current is then mirrored at the MP2 transistor because of the different gate-source voltages of the NMOS and PMOS pair of transistors

At the PMOS-transistor pair side,

$$V_{sg2} > V_{sg1} \quad results\ in \quad I_2 > I_1 \tag{4.1}$$

where $$V_{sg2} = R_p (I_{cut} + I_1) + V_{sg1}. \tag{4.2}$$

The current flowing through the PMOS transistor operating in the saturation mode is given in (4.3):

$$I_{dp} = \frac{1}{2}\mu_p C_{ox} \frac{W}{L}(V_{sg} - V_{tp})^2 \tag{4.3}$$

To operate in the saturation mode, the transistor must satisfy the following condition:

$$V_{sd} \geq V_{sg} - |V_{tp}| \tag{4.4}$$

At the same time, on the NMOS-transistor side, the voltage drop on Rn disbalances the MN3/MN4 pair. When the MP2 is passing more current, the MN4 transistor closes to channel the excess current Iout to a current output:

$$V_{gs3} > V_{g4} \quad results \quad in \quad I_{TN3} > I_{TN4} \tag{4.5}$$

where $$V_{gs4} = V_{bias} - R_n (I_{cut} + I_2) \tag{4.6}$$

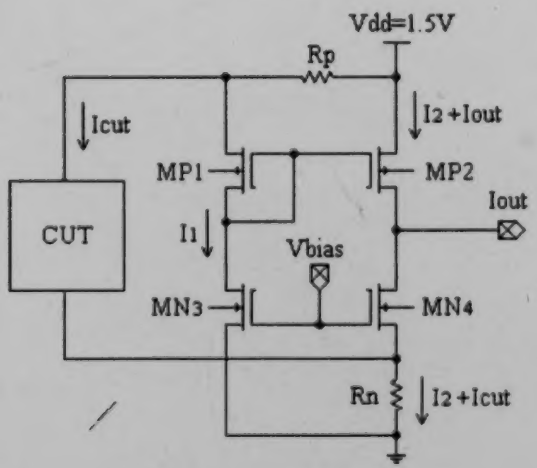

Figure 4.2: Current mirror schematics

The values of Rp and Rn are crucial for the monitor design. Earlier proposed designs [4,5,6], like the Monitor 1 design, use only one resistive element for current sensing. In contrast, Monitor 2 is uses a second current-sensing element, which will improve current monitor characteristics. As mentioned earlier the second sensing element, Rn, has two functions. The first is to improve the current's mirror response to the Icut signal. The Rn's second function is to partially control the mirror offset current resulted in conditions that disbalance the mirror, by controlling the biasing of the MN4 transistor.

The value of Rp and Rn were selected to obtain the maximum disbalance of the current mirror and, consequently, to produce a higher Iout signal. Several criteria were used to determine Rp and Rn values:

- the supply voltage degradation produced during transient current peaks ($I_{peakmax}$) is less than 5%, i.e., $I_{peakmax}(R_p+R_n) < 0.05\ V_{dd}$.
- MP1 and MN4 should be always in saturation, i.e., $V_{gs1,4} < V_{ds1,4} + V_t$.
- the Rn value should be low in order to avoid the ground-bouncing problem

The second most important parameter of the design is the value of capacitor C. Instead of amplifying the Iout, as proposed in earlier design [4], a small value of C is used (less than 500 fF), resulting in Vc signal of up to 1V. The use of a small value of C has the advantage of a faster charging and discharging time, which increases the overall speed of the monitor, and also reduces the chip area.

As was mentioned previously, in the absence of an Idd current flow, the Iout should be zero. Disbalanced PMOS transistors pass different current values even when Idd = 0, as a result of a V_{Rp} voltage drop, and produce an offset current–Ioffset. This offset current presents a problem in the design of the current mirror. The Ioffset is in the order of the milliamps and presents a mask for small leakage currents of the digital CMOS circuits (in the order of tens of nA). In order to solve this problem, the width of transistor W_{MN4} is increased from 5.0 μm to 5.1 μm, so that this offset current can be drained to the ground and removed from the Iout signal (see Figure 4.3):

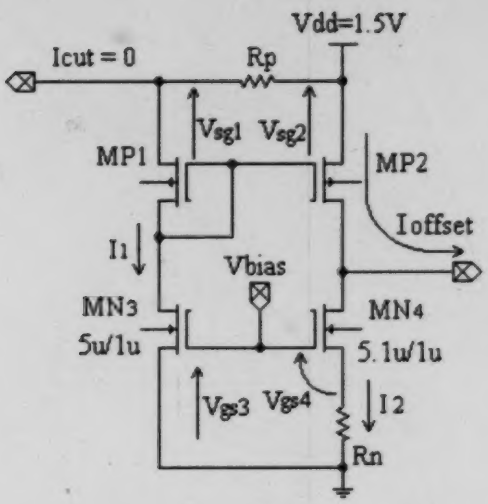

Figure 4.3: Offset current

4.3 Simulation results

The performance of the Monitor 2 was tested on two circuits: a digital circuit consisting of an 8-bit multiplier for unsigned numbers (Figure 4.4), and second circuit a mixed-signal circuit, consisting of an A/D converter feeding a 4-bit digital multiplier (Figure 4.5). The schematics of the multiplier used in the CUT design is shown in Figure 4.6. The same structure was used in a design of an 8-bit multiplier used as a digital CUT. The simulation results for two circuits are presented in Section 4.4.1 and Section 4.4.2, respectively.

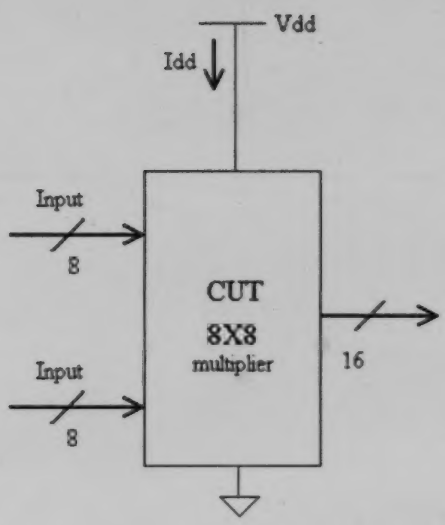

Figure 4.4: Digital circuit under test

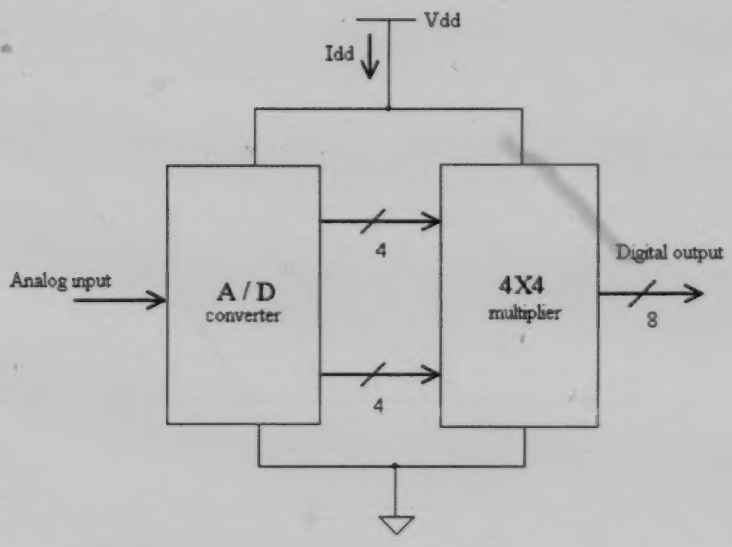

Figure 4.5: Mixed-signal circuit under test

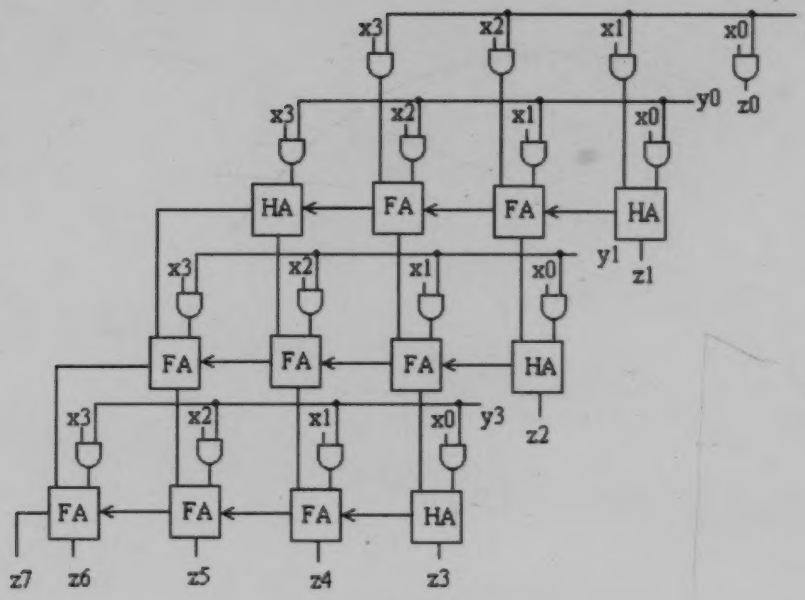

Figure 4.6: 4-bit multiplier for unsigned numbers

4.3.1 Testing of Digital Circuits

The simulation of the proposed design is first performed on an 8-bit multiplier. This circuit produces $Ipeak_{max}$ ~ 3 mA. Therefore, by using the criteria of a 5% voltage supply degradation, value of 25 Ω can be used for Rp+Rn. Because Rp has a greater effect on circuit response, its value was set to a 20 Ω and value of Rn to 5Ω. Also, low Rn value was selected to avoid the ground bouncing effect. The capacitor used in this simulation was 300fF.

The first simulation run used a circuit without a fault. The current response and the Vc signal are shown in Figure 4.7. Higher Vc responses on Iddt are distinguishable from the small Vc~Iddq responses. The uniform values of Iddq pulses indicate the absence of elevated leakage current (Vcq=83 mV). The second simulation run was done with a activated by inserting a resistive short fault between two conductive paths. Statistically, most of the shorts have resistance less than 500Ω, the value used for Rshort. The current response of the circuit with the active fault is given in Figure 4.8, which

reveals the elevated Iddq response (Vcq=146 mV) for first two and last two sets of inputs. As well, the Iddt responses caused by the fault have changed for the first three and last two sets of inputs.

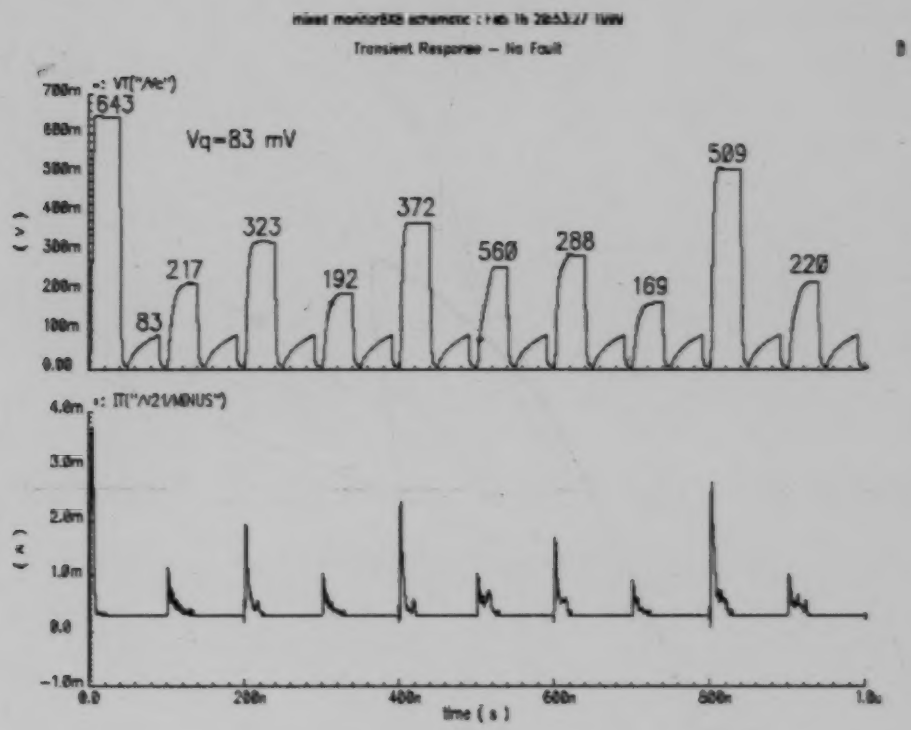

Figure 4.7: No fault response (top-Vc, bottom-Idd)

If the Iddq response were to escape the fault detection, the Iddt response would certainly not miss the fault detection or vice-versa. This result was the original reason for implementing the circuit to use both testing techniques and achieve better testing reliability.

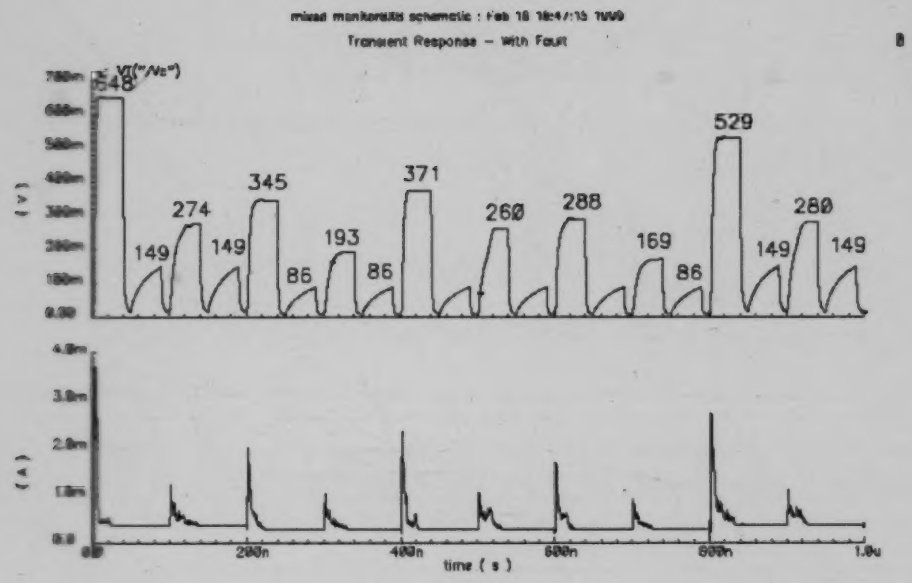

Figure 4.8: Fault response (top-Vc, bottom-Idd)

The main drawback of the Iddq testing is testing speed. The Iddq value can not be sensed before the Iddt element has settled down. For our multiplier, the transient-settling time was 27 nsec. With such a long settling time the maximum possible testing speed for concurrent Iddq/Iddt testing was 20 MHz. A higher testing speed can be achieved only by monitoring the Iddt. Since we do not have to wait for the current to settle down, but have only to pick up the initial value of the transient current pulse, a testing rate of 50 MHz can be achieved (relatively high due to the long settling time of transient current in this 8-bit multiplier).

4.3.2 Testing of Mixed-Signal Circuits

The CUT chosen for this testing consisted of an A/D converter and a 4-bit multiplier connected to the output of the converter. The procedure called "Time-domain-analysis,"

developed for testing mixed-signal circuits, was used in this test and is explained in Section 2.4.1. The stimulus is an input sequence of pulses 0-1.5 V, frequency 1 MHz.

The CUT chosen for this testing consisted of an A/D converter and a 4-bit multiplier connected to the output of the converter. The stimulus was an input sequence of pulses 0-1.5 V, frequency 1 MHz. Monitor responses with no-fault and with short-fault can be seen in Figure 4.9 and Figure 4.10, respectively.

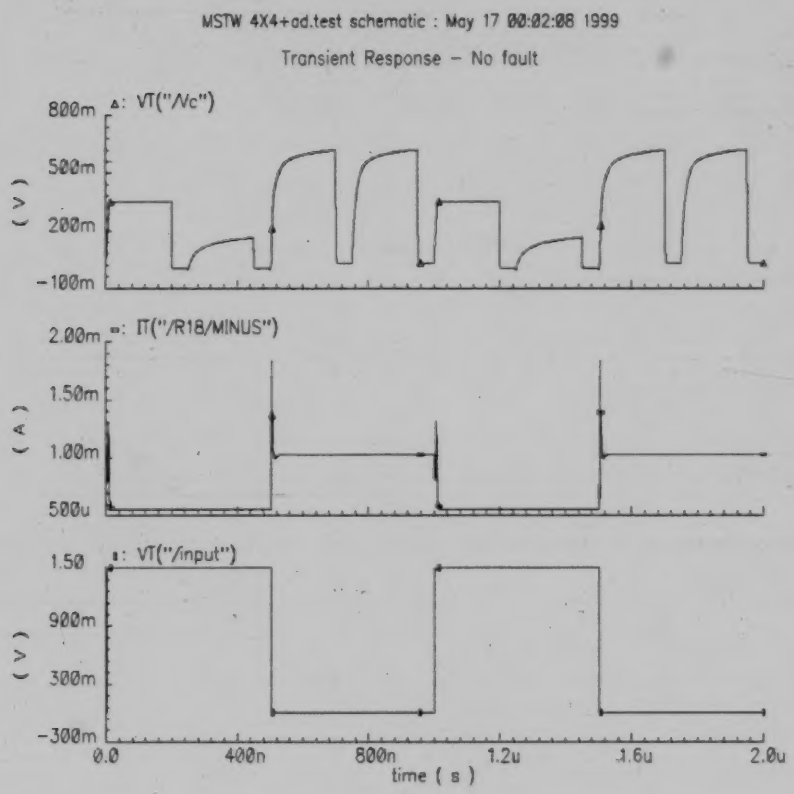

Figure 4.9: No-fault response (bottom-top: Vin, Idd, Vc)

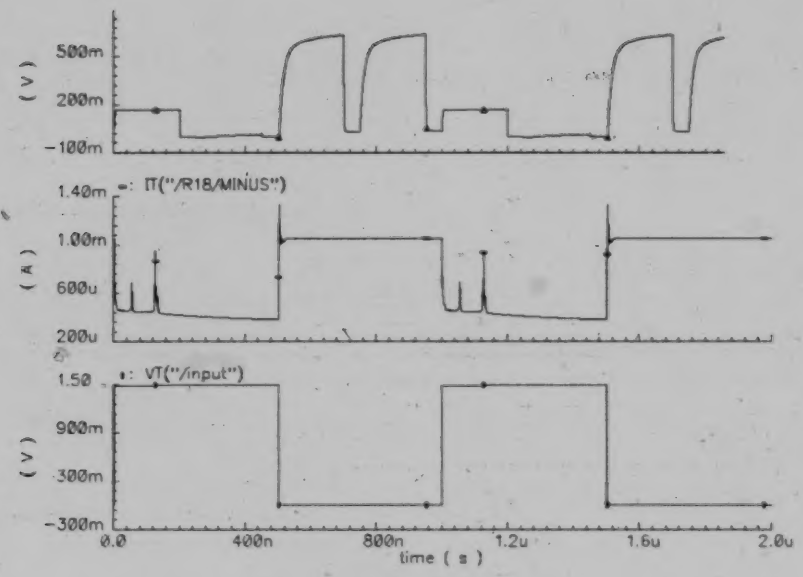

Figure 4.10: Short-fault response

(bottom-top: Vin, Idd, Vc)

In order to obtain minimum power consumption, special attention was paid to the transistor sizing and biasing of the circuit. The current through a transistor is directly proportional to its width of a transistor. The transistor widths, in current mirror and comparator designs, are selected so that power consumption of the circuit is minimized. The simulation results for the power consumption indicated that the monitor consumed less than 0.7 mW of power.

4.4 Circuit implementation

Monitor 2 circuit was implemented in 0.35 µm technology. A mixed-signal CUT was chosen for implementation as a more challenging design. The layout of the monitor with the circuit under test is shown in Figure 4.11.

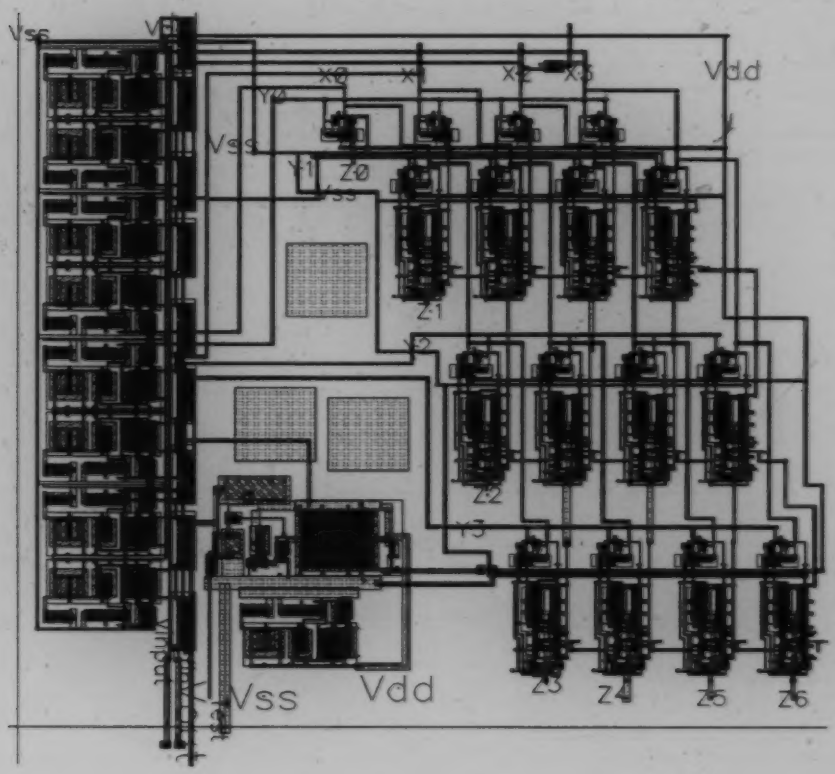

Figure 4.11: Layout of Monitor 2 with the CUT

4.5 Signal Processing

The same approach used in a processing the Monitor 1 response can be used with Monitor 2. Final output of the monitor is in digital form and easy to process and evaluate. Several options for the signal processing are described in Section 3.6.

4.6 Test Results

The same test environment, used in testing of the Monitor 1 circuit, was used in testing of the Monitor 2. The input signal was a square wave signal, 0 – 1.5 V, as required for the "time-domain analysis." The circuit did not give the expected results. There could be several reasons for that. Models used in the design of the circuit were 3.5 V models, and supply voltage used for the Monitor 2 was 1.5 V. Input signal obtained from the voltage generator had long rising and fall time, which could possibly affect the operation of the circuit. Limitations of the testing equipment could serously affect the Monitor 2 performance, since the Monitor 2 is more sensitive then the Monitor1. Though, exact reasons have yet to be determined.

Chapter 5

Critical Analysis and Future Developments

The thesis presents design of two built-in current monitors intended for on-line testing VLSI circuits. The presented work has several limitations. Some limitations are result of the limitations of monitor design itself, other dictated by the conditions in which the research work has been performed.

Both monitors require 15 % area overhead. Limitations in operating speed (less then 100 MHz) render these monitors inapplicable for the testing of high speed VLSI circuits (in the range of GHZ). Large circuits have to be partitioned in order to limit the power supply current. Also, monitors cannot detect very narrow Iddt peaks (less then 300 ps). Equipment used in testing of both designs prevented obtaining more relevant results. Long interconnection lines introduced high parasitics and made testing of the circuits almost impossible. The nature of the design process did not allow for the systematic analysis of the monitor performance in detecting different types of faults. Only two types of faults, open and short fault, were implemented and tested on the monitor. Also, long design cycles required for each fabrication run presented the time constrains during the research.

Nevertheless, the encouraging results obtained from the simulation and test results demonstrate the need for further research in current monitoring. The further developments are based on two ideas. The first is an original idea to apply an inductive sensor in current monitoring. Section 5.1 presents this new application and discusses potentials of this approach. Also in this section, a new design of the inductive element using two metal layers is described. The second topic is the development of a diagnostic module that would be used in monitoring important parameters in an IC. This material is present in Section 5.2.

5.1 Inductive Element in Current Monitoring

Until now, only resistive and capacitive elements have been used in sensing voltage-supply current. What follows is a new idea for using the inductive element and monitor the current signal by two inductive-coupled elements. Figure 5.1 illustrates inductive monitor's basic principle. The primary coil (N1) is connected in series between the circuit under test and the power supply. Changing power-supply currents induce magnetic field, sensed by the secondary coil (N2). The output voltage (Vm_1)or the output current (Im) can be monitored and the power-supply current evaluated. In order to minimize the monitor's effect on CUT, the inductor must have minimum impedance. This can be obtained with application of only a few spiral elements of the inductor. The output signal can be amplified by changing the ration between the primary and secondary coils. The relationship between the coil ratio and input/output voltages and input/output currents is given in equation (5.1). Ratio between the coil numbers in a primary and secondary coil (N1/N2) is equal to the ratio between the primary and secondary voltage (Vm1/Vm2) and between the secondary current and voltage supply current (Im/Idd).

$$\frac{N_1}{N_2} = \frac{V_{m1}}{V_{m2}} = \frac{I_m}{I_{dd}} \qquad (5.1)$$

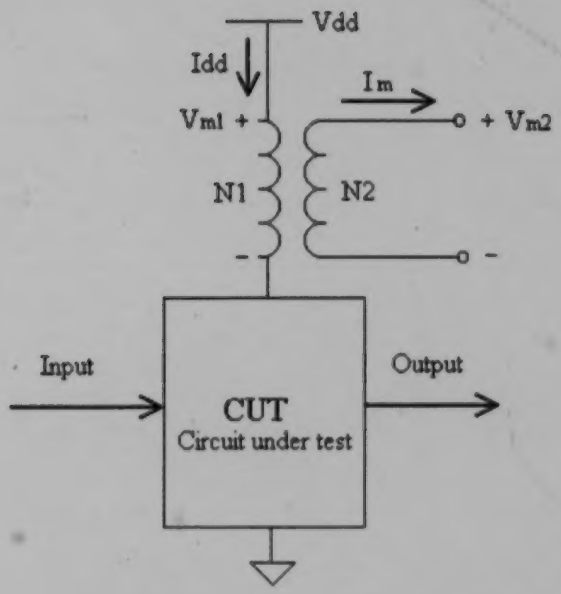

Figure 5.1: Inductive element as a current sensor

Traditional inductor design in microelectronics is based on a spiral inductor design. The main drawback is the large silicon area required, a problem prompting a new inductor layout design. The proposed inductor's layout is based on a solenoidal shape. In the same way as the wire would be coiled up, metal2 and metal3 interconnection layers were shaped. This new design is shown in Figure 5.2. Metal2 and metal3 layers are connected through the VIA23.

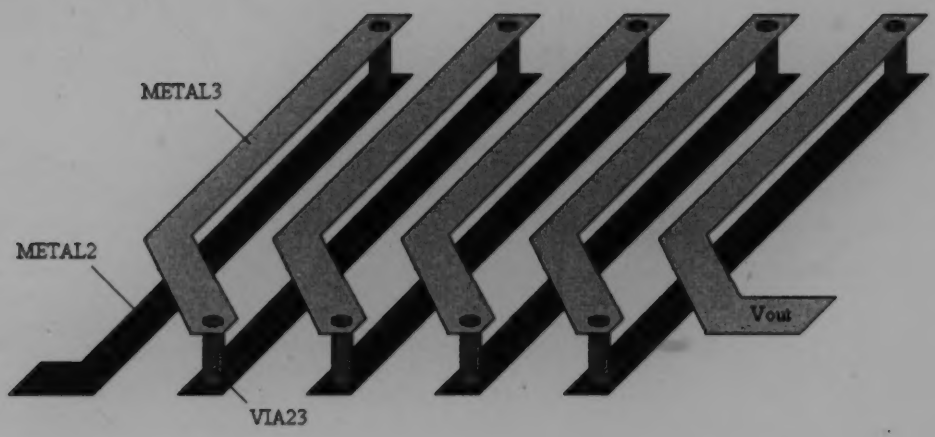

Figure 5.2: The new inductor layout design

The transformer used in picking up the current signal is based on this idea. Figure 5.3 illustrates the top view of the transformer. Two inductors are inserted, one between the other in a leather style to form a coupling pair.

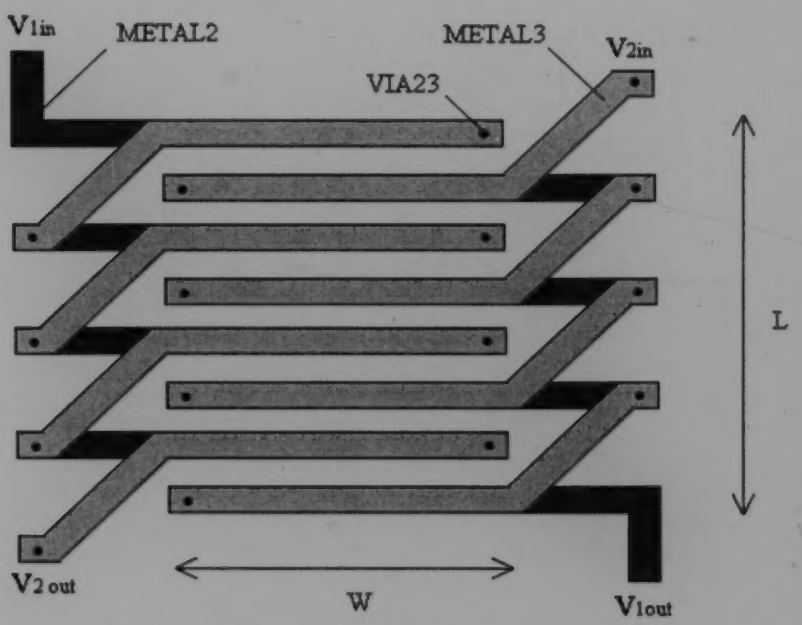

Figure 5.3: Transformer layout design

5.2 Diagnostic Module

The goal of this research would be the development of a diagnostic module to be used in testing of VLSI circuits. The current monitor part, presented in this thesis, will be used in the module design. Currently, fast low-voltage monitors for temperature and frequency evaluation are under construction.

The diagnostic module would be responsible for monitoring all the most important parameters of the integrated circuit. It would contain embedded current monitors temperature monitors, delay analyzers, frequency analyzers and a memory block. The diagnostic module scheme is illustrated in Figure 5.4.

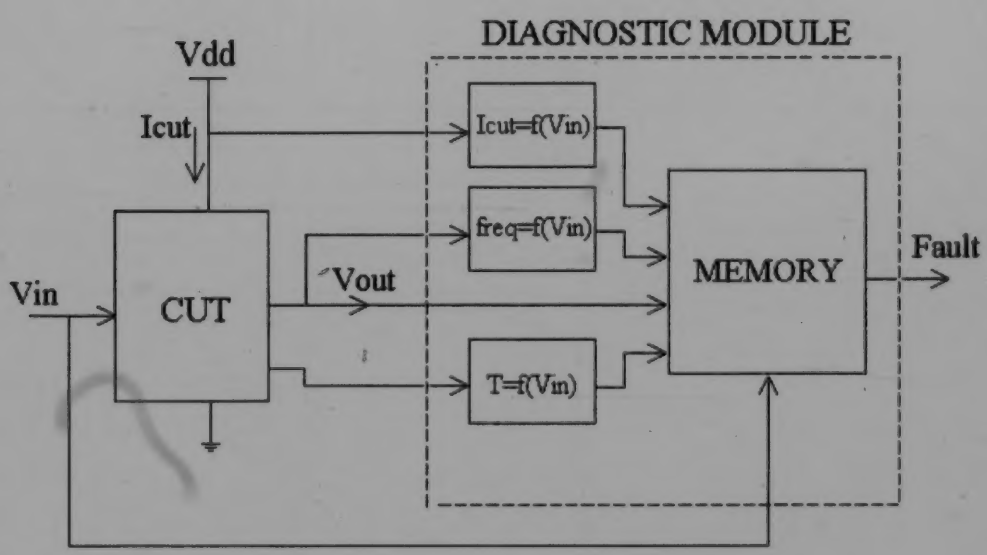

Figure 5.4: Diagnostic module scheme

The memory block stores reference information about voltage, current, temperature, frequency and delay response. This response is a function of an input signal. After comparison of the current and reference value, a Fault/No-fault signal is produced. This methodology solves the problem of low external bandwidth since all the information is

processed at rated speed inside the chip. For large circuits-under-test, a matrix of diagnostic modules is placed across the entire chip area to monitor the most active, power-dissipating sub-system units. The complete testing and diagnostic module will be not capable only of detecting and examining the faults, but also of reporting on-line status of the most critical parameters.

Chapter 6

Conclusion

The testing of VLSI circuits continues to gain importance in the manufacturing of integrated circuits. The cost associated with the VLSI testing already exceeds 50 percent of the total manufacturing cost. As well, the constantly increasing complexity of the IC's because of the new developing technologies requires the development of new techniques in IC testing.

Several problems related to the IC testing have emerged in the last few years. Increased circuit complexity, resulting from decreased device geometries, leads to the fabrication of high-density integrated circuits. Increased complexity also increases the possibility of producing faulty devices. With decreased geometries, other process parameters are scaled accordingly, including supply voltage. Low-voltage /Low- power design adds a new dimension to the testing of VLSI circuits. When a supply voltage is scaled below 2 Volts, the testability of the circuit becomes a problem. According to the International Roadmap of Semiconductors, a rapid increase in the number of transistors per pin will result in a rapid decrease in the accessibility of transistors from the chip pins, setting new limits to the IC testing. The performance of chips designed by new technologies is also rapidly increasing. The gap between the internal speed of the chip and the I/O's speed also constantly increases. These are the most important elements in

the field of the VLSI testing that require quick and efficient solutions for the emerging problems.

The limitations in traditional stuck-at fault testing methodologies show the necessity for more efficient testing approaches. Also, certain physical defects resulting from the manufacturing process cannot be modeled with existing fault models, and a new testing approached had to be found, especially for short and bridging faults. More then a decade ago, a new technique of power-supply current monitoring has showed to be very effective in detection of these types of faults. Many current monitoring techniques, as well many designs of current monitors, have been proposed in the literature of the last several years. Most of them are based on monitoring the static (quiescent) part of the power supply current. Monitoring the dynamic (transient) part of the power-supply current is still an research subject because of the difficulty of developing efficient current monitors that would be able to monitor fast-changing high-value transient current peaks. Even though current monitoring can be done externally, the most efficient approach is to develop embedded or built-in current (BIC) monitors in order to allow at-speed testing avoiding the speed limitations of the I/O's. Additionally, BIC monitors provide the possibility for on-line testing performed during the normal operation of the tested circuit.

This thesis has presented the work in the developing of two BIC monitors used for on-line testing. Same monitors were developed for testing transient and quiescent power-supply current. Monitors were designed for a low-voltage environment (1.5 Volts power-supply). Both can be used in testing battery-operated circuits and Low-Power/Low/Voltage devices.

The first monitor, Monitor 1, is the improved design of the Stopjaková/Manhaeve monitor. An interconnecting metal layer, used as a current sensing element, was substituted for the resistor, increasing sensitivity of the current monitor. As well, the impact of the current monitor on the circuit-under-test could be varied, according to the design requirements. A new feature of Monitor 1 was the addition of a fast analog to digital (A/D) converter. Converting the output signal of the monitor to a digital signal creates the advantage of easier processing of the monitor response. The performance of the monitor design was first confirmed through the simulation of the current monitor applied to the sets of inverters, as the circuit-under-test. Next, the monitor was

manufactured with the cooperation of the Canadian Microelectronics Corporation (CMC) by Taiwan Semiconductor Manufacturing Company (TSMC). Monitor 1 was implemented in two technologies, 0.5 μm and 0.35 μm. A test-bench was set for testing manufactured designs. Test results indicated the correct operation of the designed monitor. Open fault was activated by connecting the part of the circuit. The fault was successfully detected by the Monitor 1.

Monitor 2, described in the Chapter 4, is a new proposed design of the current monitor. It elaborated on the principle behind the previously proposed monitor. A second current sensing element was added to improve monitor sensitivity and performance. This monitor was intended for both transient and quiescent current monitoring. This feature enhances the testing capabilities of the monitor by using the advantages of both current monitoring techniques. Output of the monitor was also digitized on a fast A/D converter. The digital signal was easy to process and evaluate. The performance of the Monitor 2 was tested on two different CUT's. The first was a digital circuit, an 8-bit multiplier. A short fault was simulated by connecting the two interconnection lines through a resistive element. The monitor successfully detected the fault. The second CUT used with the Monitor 2 was the Mixed-signal design containing an A/D converter and a 4-bit multiplier connected to the converter's output. The mixed-signal design of the Monitor 2 was implemented in a 0.35 μm technology. Unfortunately, problems in the layout was discovered and expected test results could not be obtained.

The two current monitor designs presented in this thesis, resulted from the research on new approaches in testing VLSI circuits. Current monitoring proved a very efficient technique in detecting difficult-to-detect faults. Monitor 1 and Monitor 2 were developed for testing Low-Voltage circuits. The on-line testing capabilities of the two monitors are the main advantage of these designs. In addition, an embedded monitor design solves the problem of the gap between the internal and external I/O performance of the integrated circuit.

The work in this thesis demonstrated the need for further research in current monitoring. Both monitor designs presented in this thesis indicate the great potential of current monitoring in testing VLSI circuits.

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